Compal Confidential

B3ZMS MB Schematic Document

LA-D591P

Rev: 2.0

2016.02.24

DAX1

Part Number	Description
DAA000C2000	PCB 1JL LA-D591P REV0 MB 1

B3ZMS_PCB_REV01

Security Classification	Compal Secret Data		
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HDMI x 4 lanes

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DDI

Intel Skylake U

Skylake U
Skylake PCH-LP(MCP)
(SKL-U_2+2)

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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1(Skylake)
1	0.2(Skylake)
2	1.0(Skylake)
3	2.0(Skylake)
4	
5	
6	
7	2.0(Kabylake)

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
LPC MODE for EC	LPC@
ESPI MODE for EC	ESPI@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
For Skylake-U	SKL@
For Kabylake-U	KBL@
SPI ROM 8M*1	8M_SINGLE@
TPM	TPM@
DMIC*1	1DMIC@
For ES Sampel Only	ES@
Keyboard backlight	KB@
Finger Print	FP@

BOM Option Table

Item	BOM Structure
CODEC(ALC255)	255@
CODEC(ALC283)	283@
DRAM BOM Select	X76@/X7601@ ~ X7614@
CPU Code	
	QS:QJ8Q@,QJKK@, QJKR@,QJKP@
	MP:SR2EU@,SR2EY@

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDRIIIL +1.35V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.5VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 level BOM table

43 Level	Description	BOM Structure
431A1MBOL06	PCBA MB AD591 B3ZMS I36100U SR2EU 4G HDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EU@
431A1MBOL07	PCBA MB AD591 B3ZMS I56200U SR2EY 4GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EY@
431A1MBOL08	PCBA MB AD591 B3ZMS I56200U SR2EY 8GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EY@
431A1MBOL09	PCBA MB AD591 B3ZMS I76500U SR2EZ 4GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EZ@
431A1MBOL10	PCBA MB AD591 B3ZMS I76500U SR2EZ 8GHDMI	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EZ@
431A1MBOL11	SMT MB AD591 B3ZMS PMD4405USR2EX 4G	8M_SINGLE@/EMC@/SKL@/KB@/LPC@/IOAC@/SR2EX@

Skylake CPU

UC1 PMD4405 QJ8Q D0 2.1G BGA
SR2EX@
SA000094270

UC1 i3-6100U SR2EU D1 2.3G BGA
SR2EU@
SA000092NB0

UC1 i5-6200U SR2EY D1 2.3G BGA
SR2EY@
SA000092OB0

UC1 i7-6500U SR2EZ D1 2.5G BGA
SR2EZ@
SA000092P90

Kabylake CPU

UC1 QKKQ G0 1.7G FCBGA
QKKQ@
SA00009QM10

UC1 QKKS G0 2.4G BGA
QKKS@
SA00009PJ30

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Title: Notes List

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A4WAS Schematic: LA-C611PR01_1208.DSN

+19VB

ALW

V

VS

VR / Load SW	Power Rail Name	VR / Load SW	Power Rail Name	VR / Load SW	Power Rail Name
PU9001 NCP81253MNTBG_DFN8_2X2 EN: DRVON	+VCC_CORE				
PU9003 NCP81151MNTBG_DFN8_2X2 EN: DRVON	+VCC_GT				
PU9004 NCP81253MNTBG_DFN8_2X2 EN: DRVON	+VCC_SA				
PU501 RT8207PGQW_W QFN20_3X3 EN: SYSON	+0.675VS_VTT				
	+1.35V_VDDQ	JPC1,JPC2 JUMP	+1.35V_VDDQ_CPU	RC208 0 ohm_0402	+1.35V_VDDQC
				RC141 0 ohm_0402 (Short-Pad)	+1.35V_VCCSFR_OC
PU402 SY8286CRAC_QFN20_3X3 EN: 3SV_EN	+5VALW	U25 SY6288C20AAC_SOT23-5 EN: USB_CHARGE_2A	+USB3_VCCA		
		U26 SY6288C20AAC_SOT23-5 EN: USB_EN	+USB3_VCCB		
		U11 EM5209VF_DFN14_2X3(Dual Load	+5VS	U31 NCT3942S EN: +5VS	+VCC_FAN1
				U52 AP2330W-7	+HDMI_5V_OUT
				U66 SY6288C20AAC EN: ODD_EN	+5VS_ODD
				U10 SY6288C20AAC EN: KBL_EN	+5VS_BL
				+VDDA	+VDDA
				+5VS_HDD	+5VS_HDD
PU401 SY8286BRAC_QFN20_3X3 EN: 3V5V_EN	+3VALW	JPC7 JUMP	+3VALW_PRIM	RC154 0 ohm_0402 (Short-Pad)	+3VALW_SPI
				RC171 0 ohm_0402 (Short-Pad)	+3VALW_RTC
				RC158 0 ohm_0402	+3VALW_HDA
				RC197 0 ohm RC161 R-short RC163 R-short RC172 0 ohm RC167 R-short RC187 R-short	+3VALW_1.8VALW_PGPPA +3VALW_PGPPB +3VALW_PGPPC +3VALW_1.8VALW_PGPPD +3VALW_PGPPE +3VALW_PGPPG
		U2504 SY6288C20AAC EN: LAN_PWR_EN	+3V_LAN		
		U13 SY6288C20AAC EN: TP_PWR_EN	+3V_PTP		
		R3600 0 ohm_0603(Short-Pad)	+3VALW_TPM		
		RC173 0 ohm_0402	+3VALW_DSW		
		U9 SY6288C20AAC EN: WLAN_ON	+3VS_WLAN		
		U11 EM5209VF_DFN14(Dual Load SW)	+3VS	U12 SY6288C20AAC EN: DGPU_PWR_EN	+3VSDGPU_AON
					J14 JUMP → +3VSDGPU_MAIN
				PU1101 SY8032ABC EN: DGPU_PWROK	+1.05VSDGPU
				U8 SY6288C20AAC EN: SOC_ENVDD	+LCDVDD
				R2554 0 ohm_0603	+3VS_ALS
				L3 FBMA-L11-160808-800LMT	+3VS_CRT
				J7 JUMP	+3VS_WLAN
				R2601 0 ohm_0603(Short-Pad)	+3VS_TPM
				R470 0 ohm_0402(Short-Pad)	+3VS_DVDD
				R471 0 ohm_0402(Short-Pad)	+3VS_DVDDIO
PU701 SY8032ABC_SOT23-6 EN: SPOK	+1.8VALW_PRIM			UC5 EM5209VF EN: SUSP#	+1.8VS
				JPC8 JUMP	+1.8VALW_VS
				RC206 0 ohm_0402	+3VALW_1.8VALW_PGPPD
				RC196 0 ohm_0402	+3VALW_1.8VALW_PGPPA
PU702 APL5930KAI-TRG_SO8 EN: SUSP#	+1.5VS				

PU601 SY8288RAC_QFN20_3X3 (VR) EN: +1.8VALW_PG	+1.0VALW_PRIM	UC5 (1/2) EM5209VF (Dual Load SW) EN: SYSON	+1.0V_VCCSTU
			RC140 0 ohm_0402 (Short-Pad) → +1.0V_VCCST
			RC143 0 ohm_0402 (Short-Pad) → +1.0V_VCCSFR
		JPC9JUMP	+1.0VALW_MPHYPLL
			RC149 0 ohm_0402 (Short-Pad) → +1.0V_AMPHYPLL
			RC156 0 ohm_0402 (Short-Pad) → +1.0V_APLLEBB
			RC209 0 ohm_0402 → +1.0VALW_MPHYGT
			RC176 0 ohm_0402 → +1.0VALW_SRAM
		RC12 0 ohm_0402 (Short-Pad)	+1.0V_XDP
		RC148 0 ohm_0402 (Short-Pad)	+1.0VALW_APLL
		RC190 0 ohm_0402 (Short-Pad)	+1.0VALW_CLK4_F100OC
		RC164 0 ohm_0402 (Short-Pad)	+1.0VALW_VCCCLK2
		RC175 0 ohm_0402 (Short-Pad)	+1.0VALW_MPHYAON
		RC152 0 ohm_0603(Short-Pad)	+1.0VALW_CLK5_F24NS
		RC175 0 ohm_0402 (Short-Pad)	+3.0VALW_MPHYAON
		RC169 0 ohm_0402 (Short-Pad)	+1.0VALW_CLK6_24TBT
		UC6 TPS22961DNYR (Single Load SW) EN: SUSP#	+1.0VS_VCCSTG
PU1201 RT8812AGQW_W QFN20_3X3 EN: 3VSDGPU_MAIN_EN	+GPU_CORE		
PU1001 SY8288RAC_QFN20_3X3 EN: 1.5VS_DGPU_PWR_EN	+1.5VSDGPU		

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Title: *Power Map*

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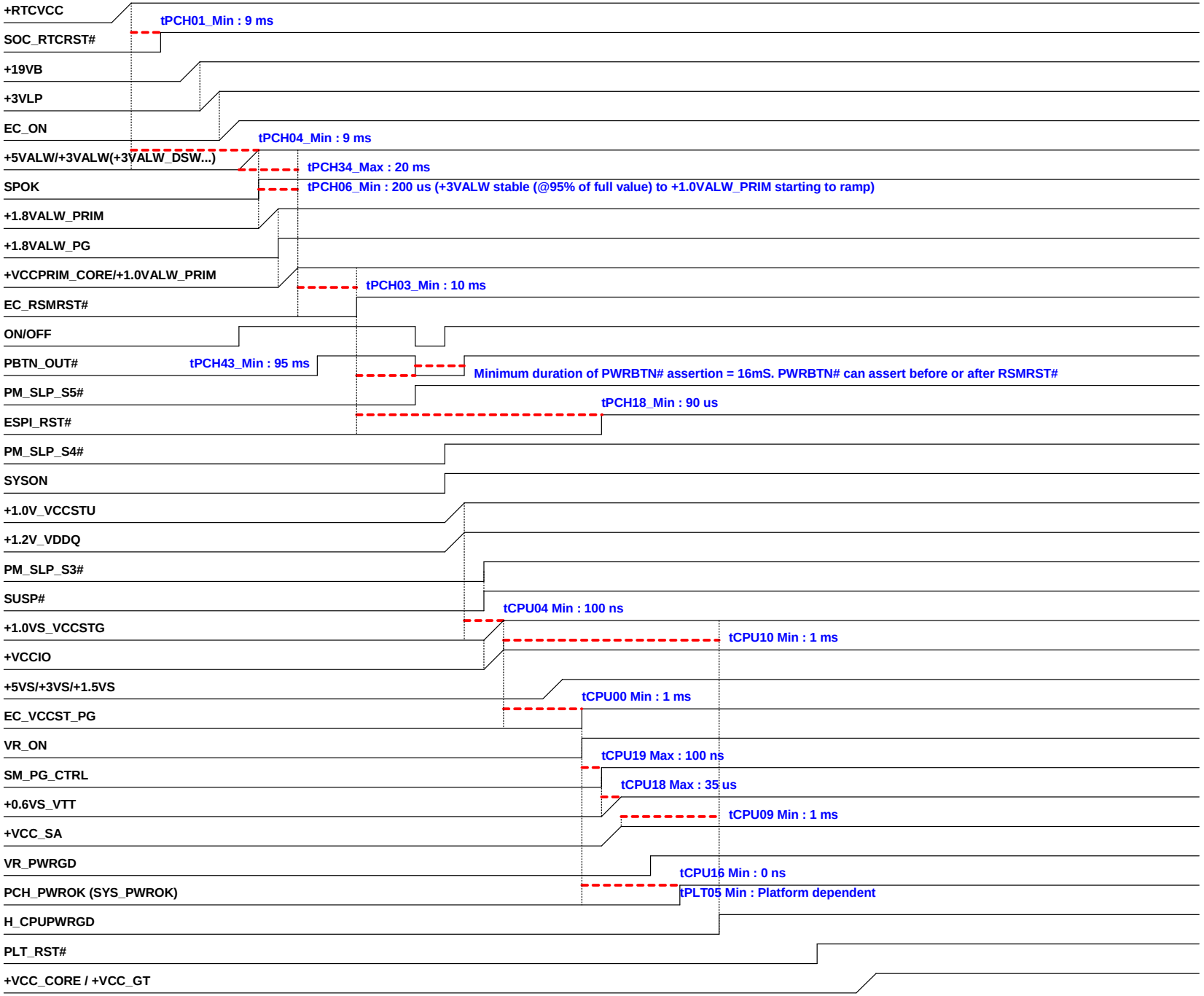
PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



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Title: Power Sequence

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SOC_DP1_CTRL_DATA(Internal Pull Down):

Display Port B Detected

0 = Port B is not detected.

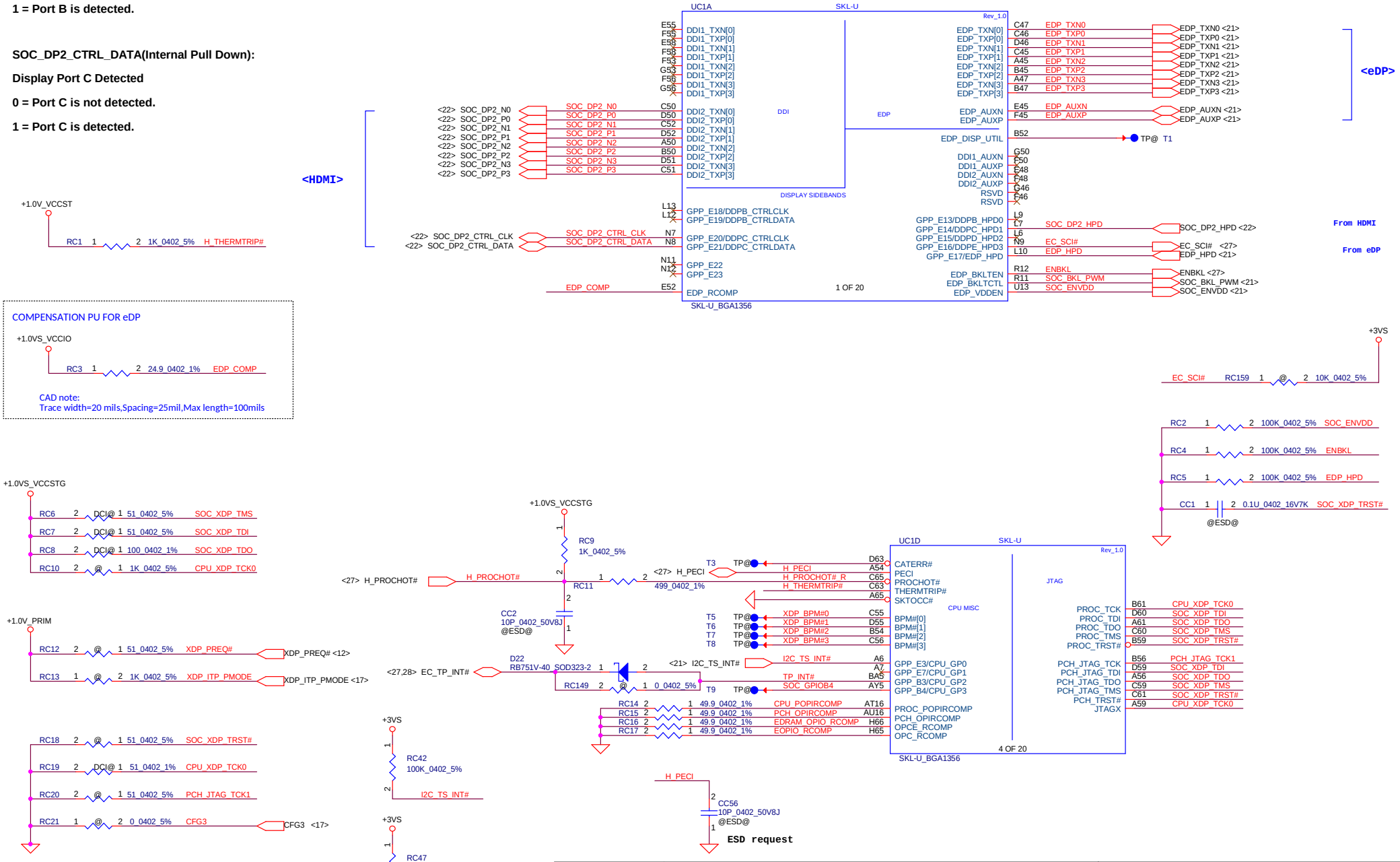
1 = Port B is detected.

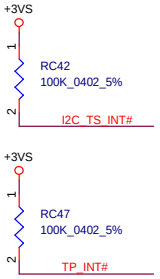
SOC_DP2_CTRL_DATA(Internal Pull Down):

Display Port C Detected

0 = Port C is not detected.

1 = Port C is detected.





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Title: **SKL-U(1/12))DDI,MSIC,XDP,EDP**

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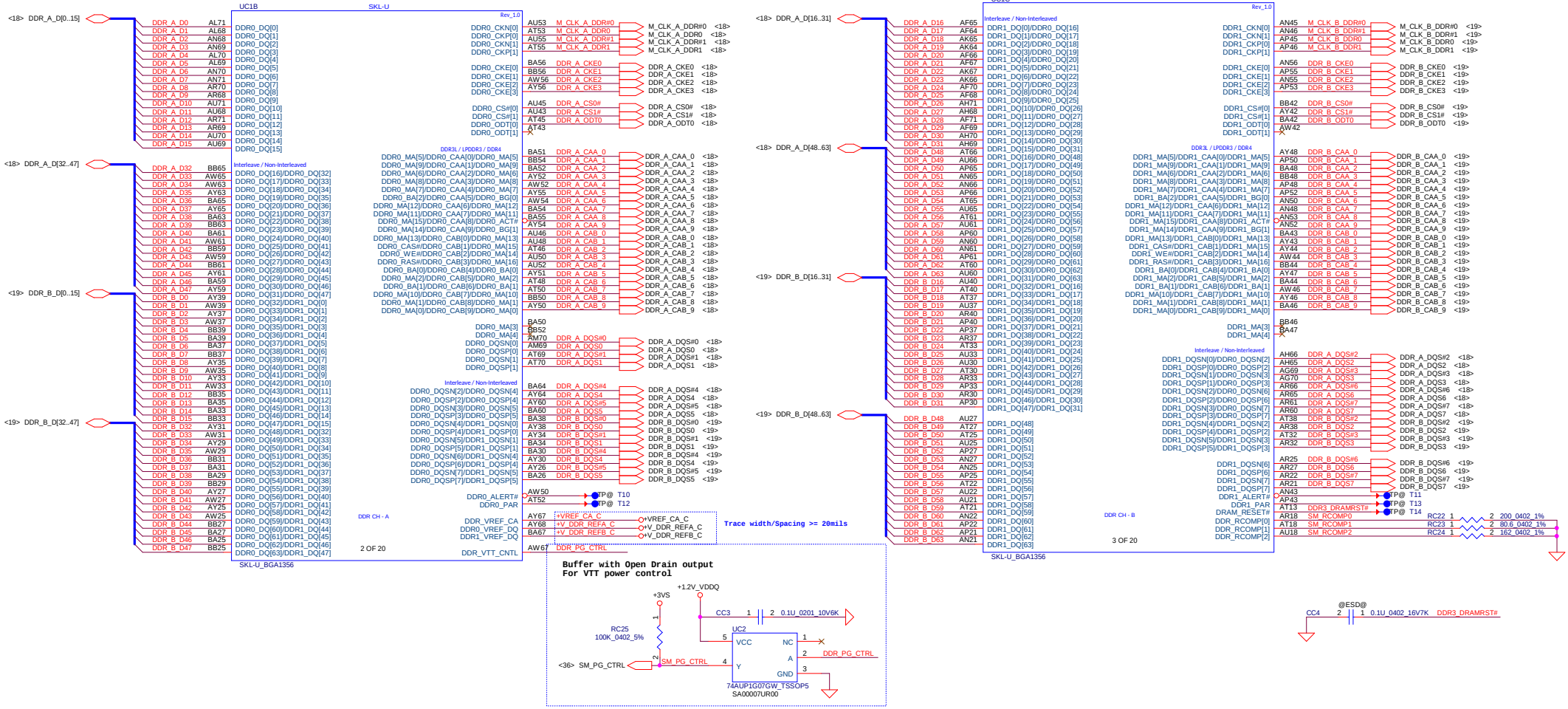
non-Interleaved

non-Interleaved



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Title: SLK-U(2/12)LPDDR3

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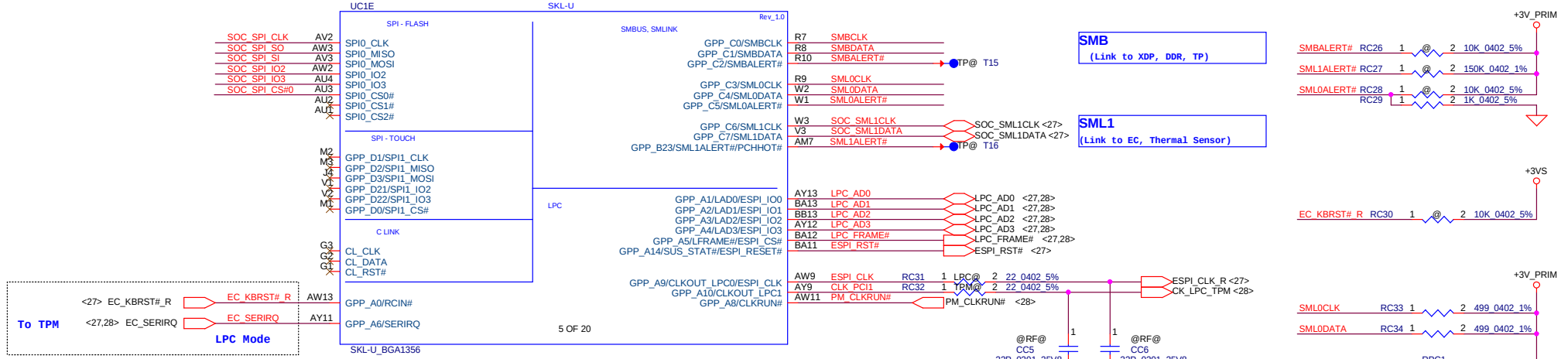
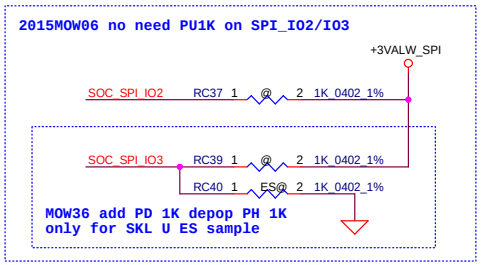
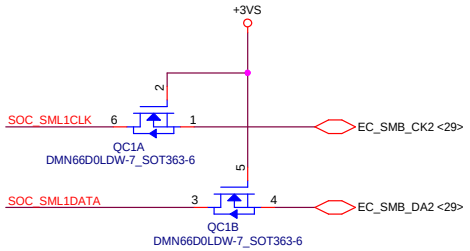
SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

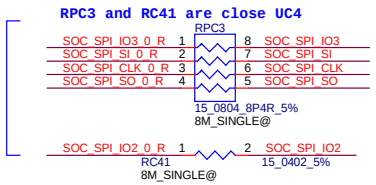




Follow 543016_SKL_U_Y_PDG_0_9

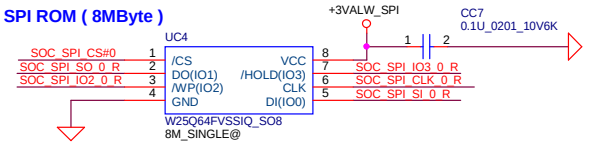


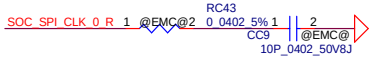
Single SPI ROM_CS0#



SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

SPI ROM (8MByte)





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Compal Electronics, Inc.

Title: **SKL-U(3/12)SPI,ESPI,SMB,LPC**

Size	Document Number	Rev
Custom	B3ZMS LA-D591P	2.0

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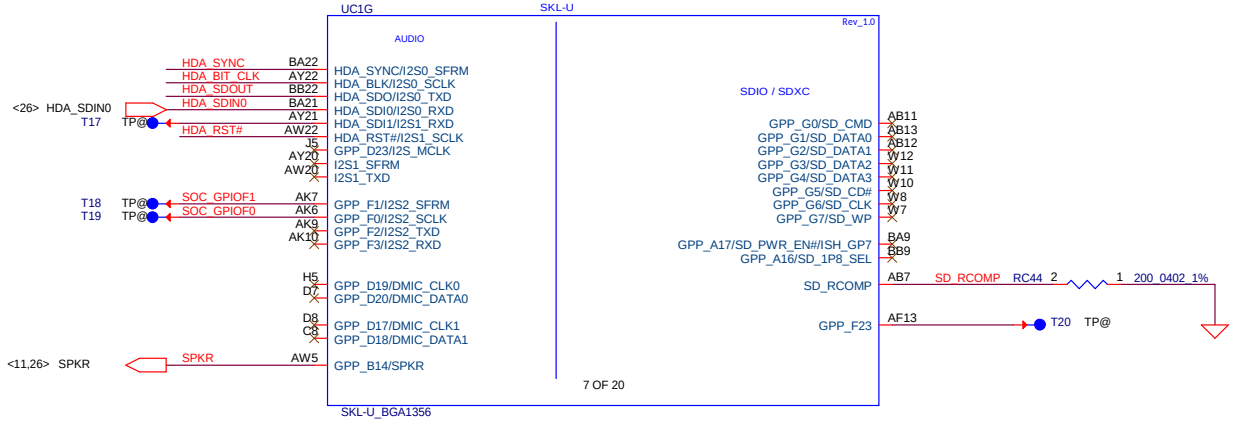
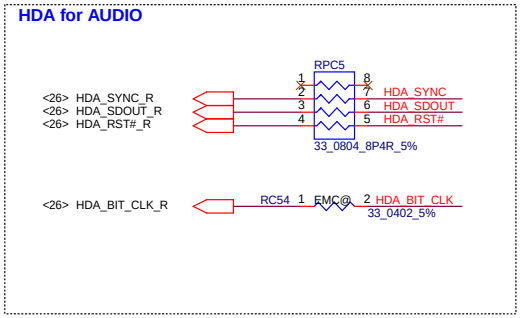
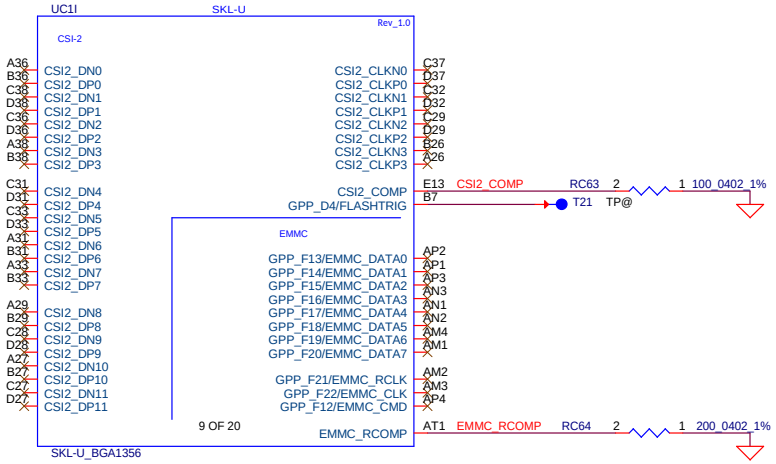


HDA for AUDIO





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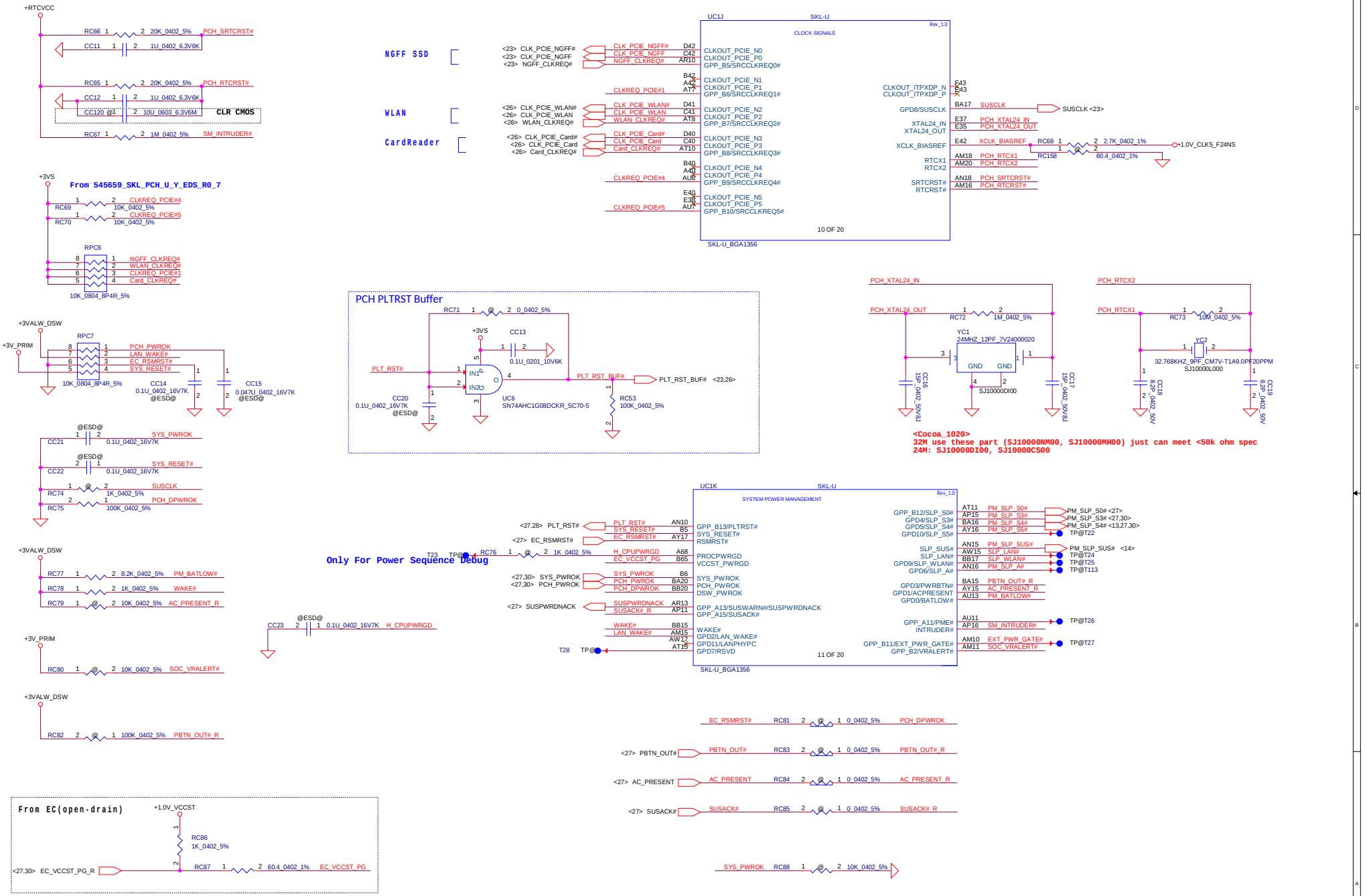
Compal Electronics, Inc.

Title: **SKL-U(4/12)HDA,EMMC,SD**

Size	Document Number	Rev
Custom	B3ZMS LA-D591P	2.0

Date: Wednesday, February 24, 2016 Sheet 9 of 45



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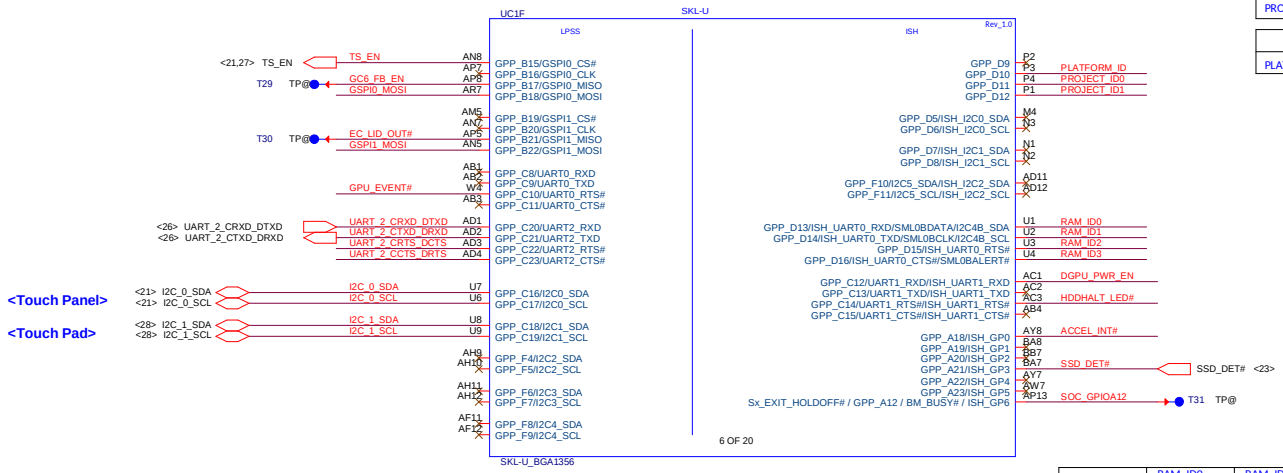
Compal Electronics, Inc.

Title: **SLK-U(5/12)CLK,GPIO**

Size	Document Number	Rev
Custom	B3ZMS LA-D591P	2.0

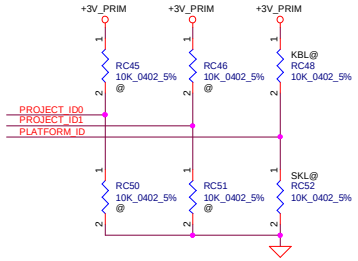
Date: Wednesday, February 24, 2016 | Sheet 10 of 45

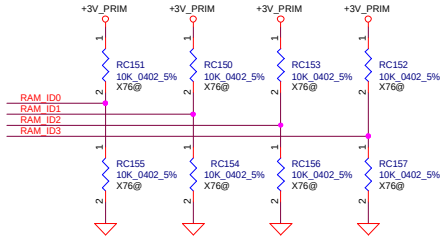


PROJECT_ID0	0	1

PROJECT_ID1	0	1

	SKL-U	KBL-U
PLATFORM_ID	0	1





	RAM_ID0	RAM_ID1	RAM_ID2	RAM_ID3	PartNumber - Description
X76669BOL01 SAM 4GB	X	X	0	0	SA00005WX60 - S IC D3 8G/1600 K4E8E304EE-EGCE ABO!
X76669BOL03 SAM 8GB	X	X	0	1	SA00005ZQ50 - S IC D3 512M32/1600 K4E6E304EE-EGCE ABO!
X76669BOL02 HYN 4GB	X	X	1	0	SA00009GZ10 - S IC D3 8G/1866 H9CCNNN8JTBLAR-NUD ABO!
X76669BOL04 HYN 8GB	X	X	1	1	SA00009H210 - S IC D3 16G/1866 H9CCNNNBLTBLAR-NUD ABO!

Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.---> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

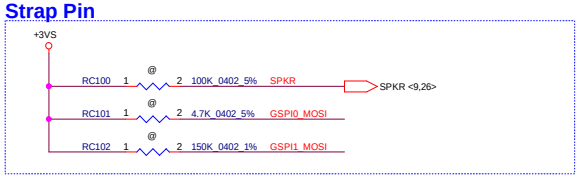
GSPI1_MOSI (Internal Pull Down):

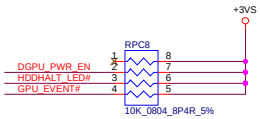
Boot BIOS Strap Bit

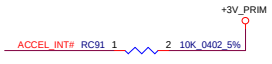
0 = SPI Mode --> AAX05 Use

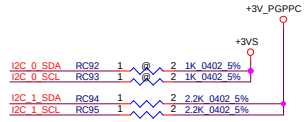
1 = LPC Mode

Strap Pin









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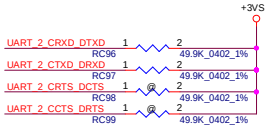
Follow #544669 GPIO I/O setting



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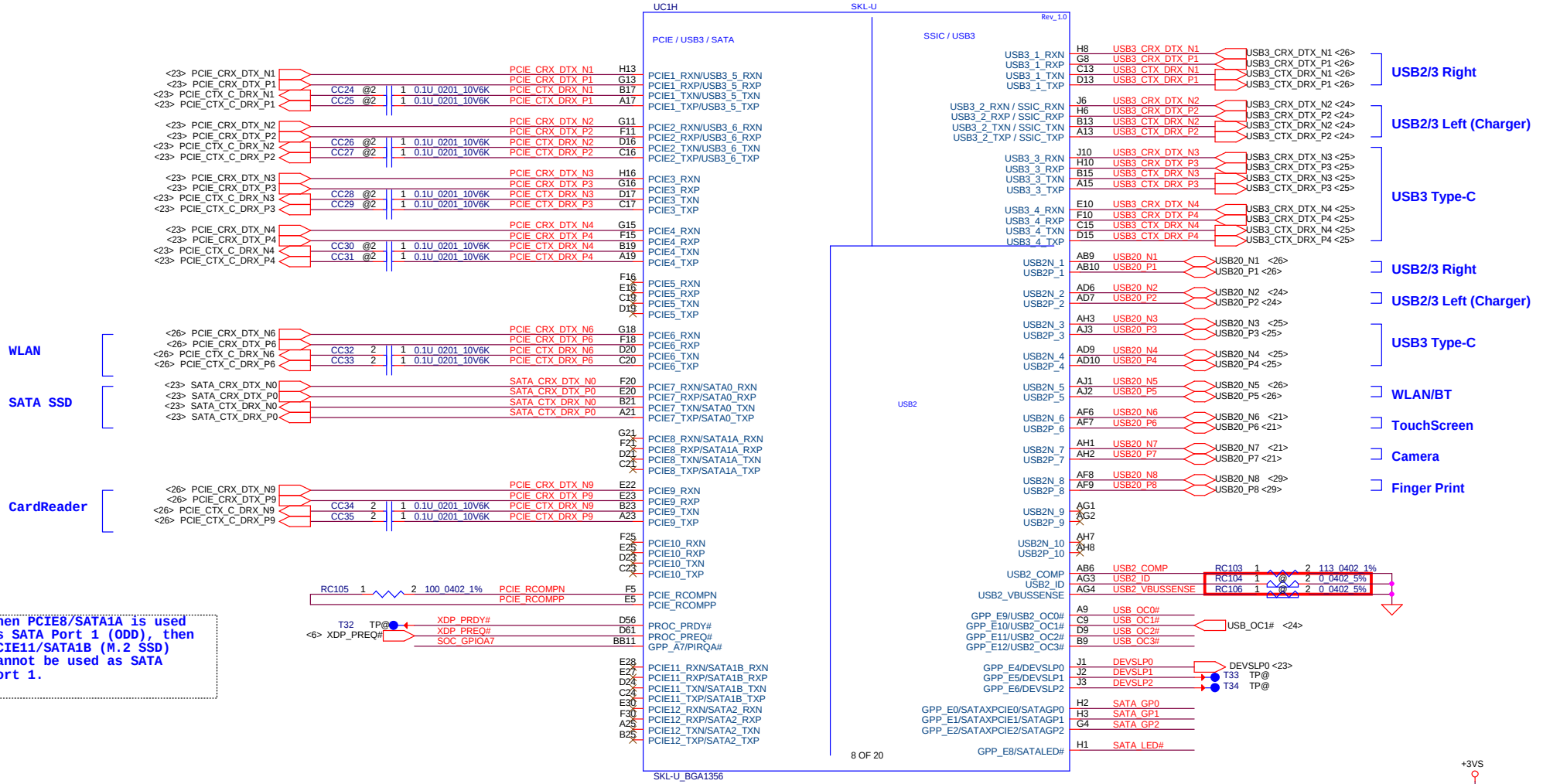
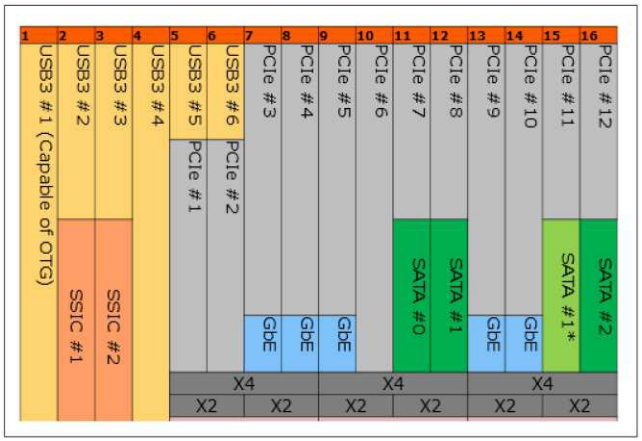
			Date: Wednesday, February 24, 2016; Sheet 11 of 45



High Speed I/O (HSIO) Lane Multiplexing in SKL U



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1&2
USB_OC1#	USB2 Port 3
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NGFF SSD KEY B
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

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Issued Date	2015/10/21	Deciphered Date	2016/06/21

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Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

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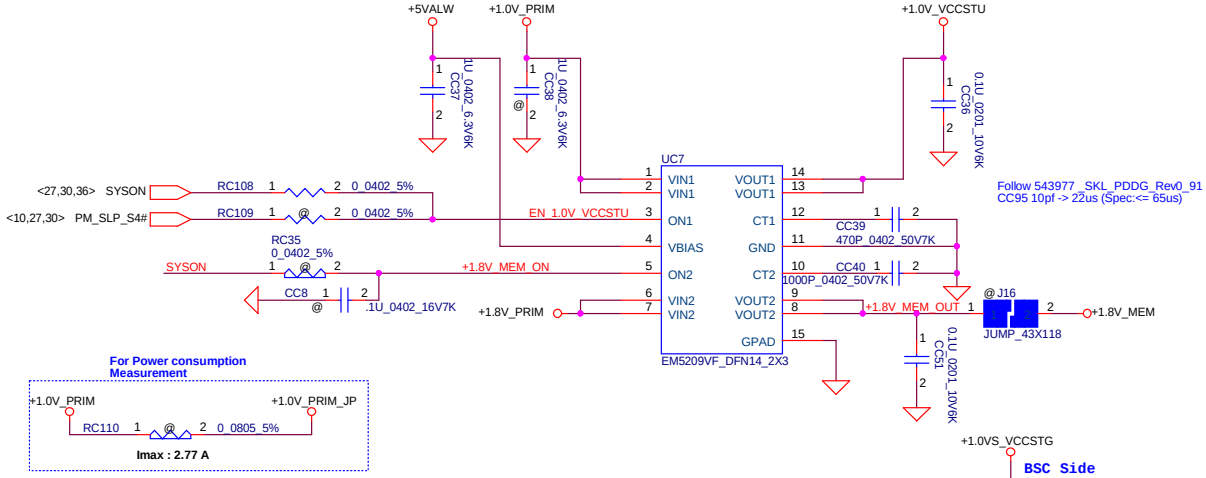
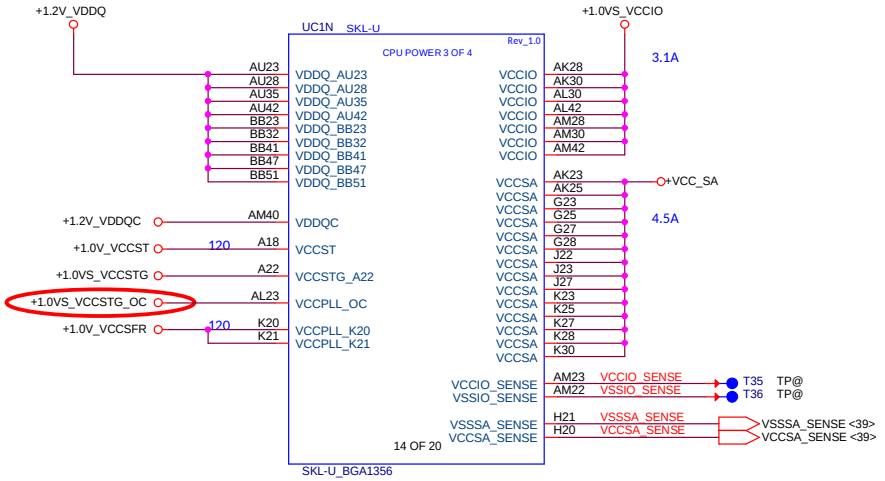
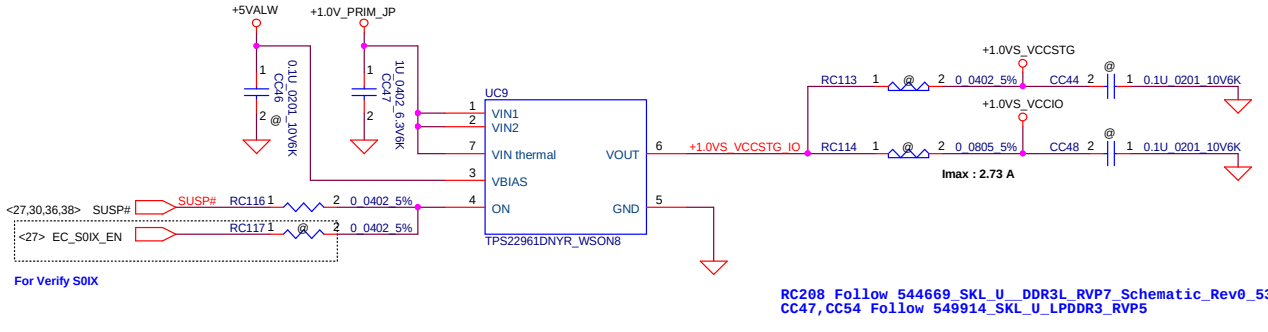
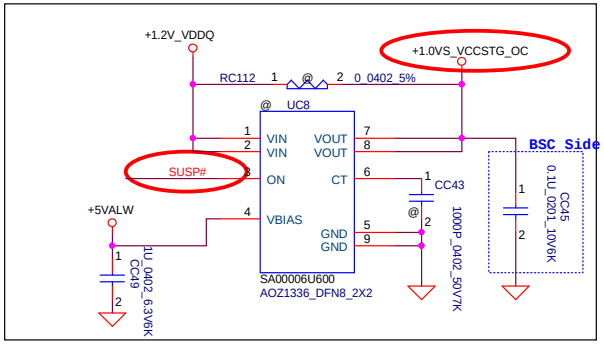
+1.0V_PRIM TO +1.0V_VCCSTU



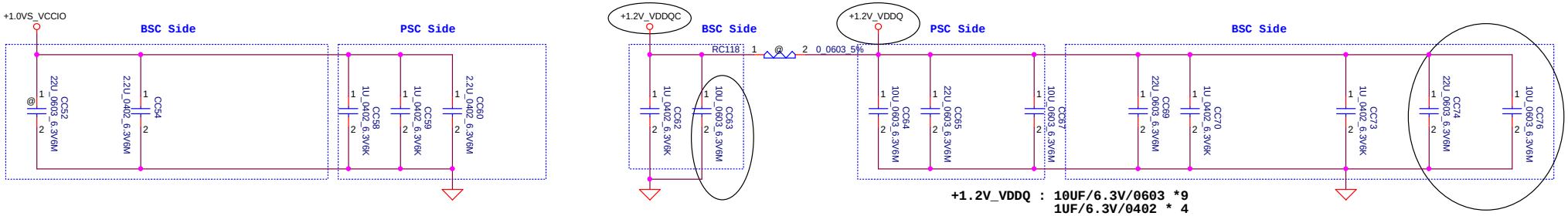


+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO





RC208 Follow 544669_SKL_U__DDR3L_RVP7_Schematic_Rev0_53
CC47,CC54 Follow 549914_SKL_U_LPDDR3_RVP5



+1.2V_VDDQ : 10UF/6.3V/0603 *9
1UF/6.3V/0402 * 4

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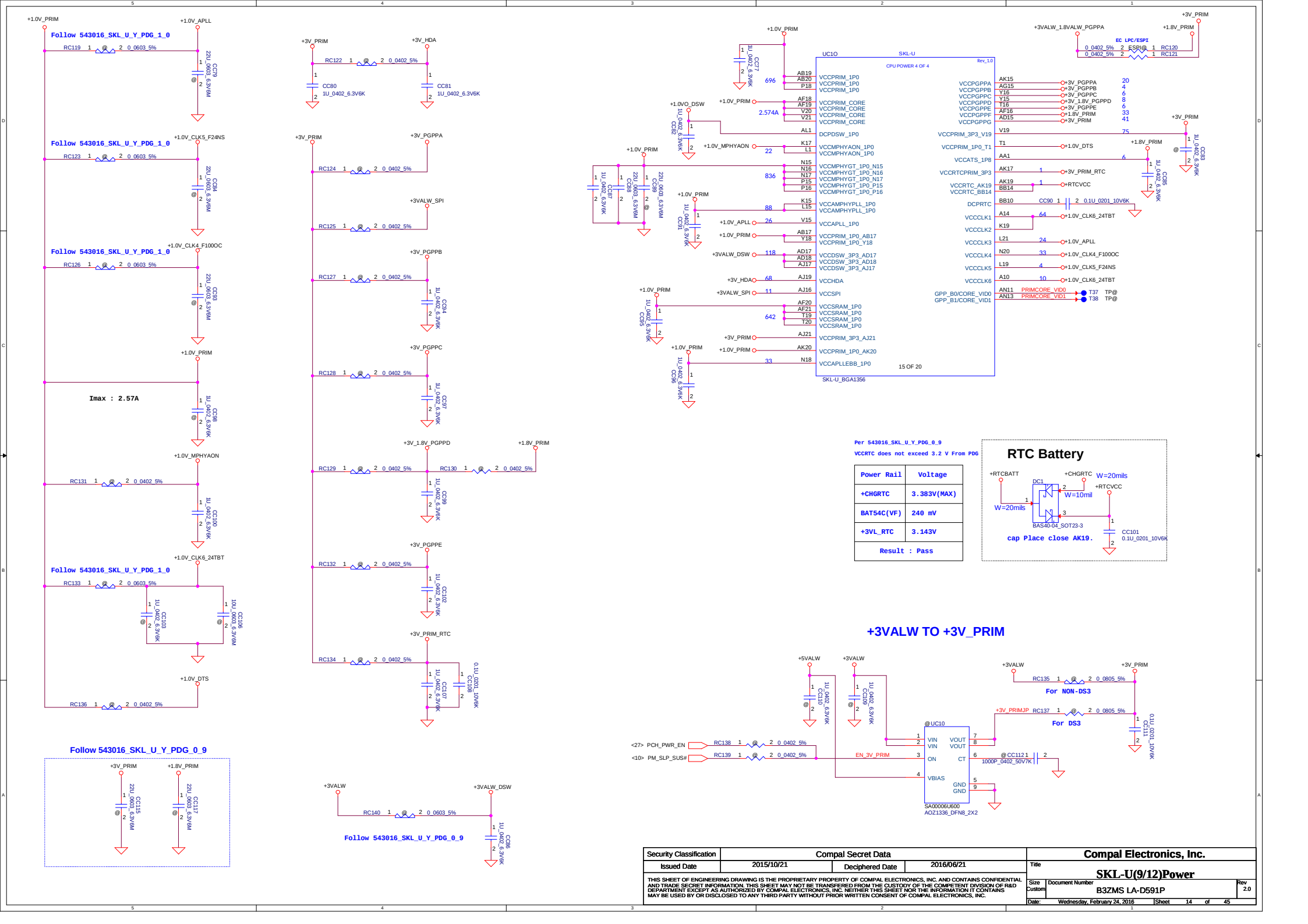
Title: SKL-U(8/12)POWER			
Size: Custom	Document Number: B3ZMS LA-D591P		Rev: 2.0
Date: Wednesday, February 24, 2016	Sheet 13 of 45		


Follow 543016_SKL_U_Y_PDG_1_0
Follow 543016_SKL_U_Y_PDG_0_9
Imax : 2.57A
UC1O
SKL-U
CPU POWER 4 OF 4
Rev_1.0
15 OF 20
SKL-U_BGA1356
Per 543016_SKL_U_Y_PDG_0_9
VCCRTC does not exceed 3.2 V From PDG
Power Rail | Voltage
+CHGRTC | 3.383V(MAX)
BAT54C(VF) | 240 mV
+3VL_RTC | 3.143V
Result : Pass
RTC Battery
cap Place close AK19.
+3VALW TO +3V_PRIM
For NON-DS3
For DS3
Follow 543016_SKL_U_Y_PDG_0_9
Security Classification | Compal Secret Data
Issued Date | 2015/10/21 | Deciphered Date | 2016/06/21
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SKL-U(9/12)Power
B3ZMS LA-D591P
Rev 2.0
Wednesday, February 24, 2016
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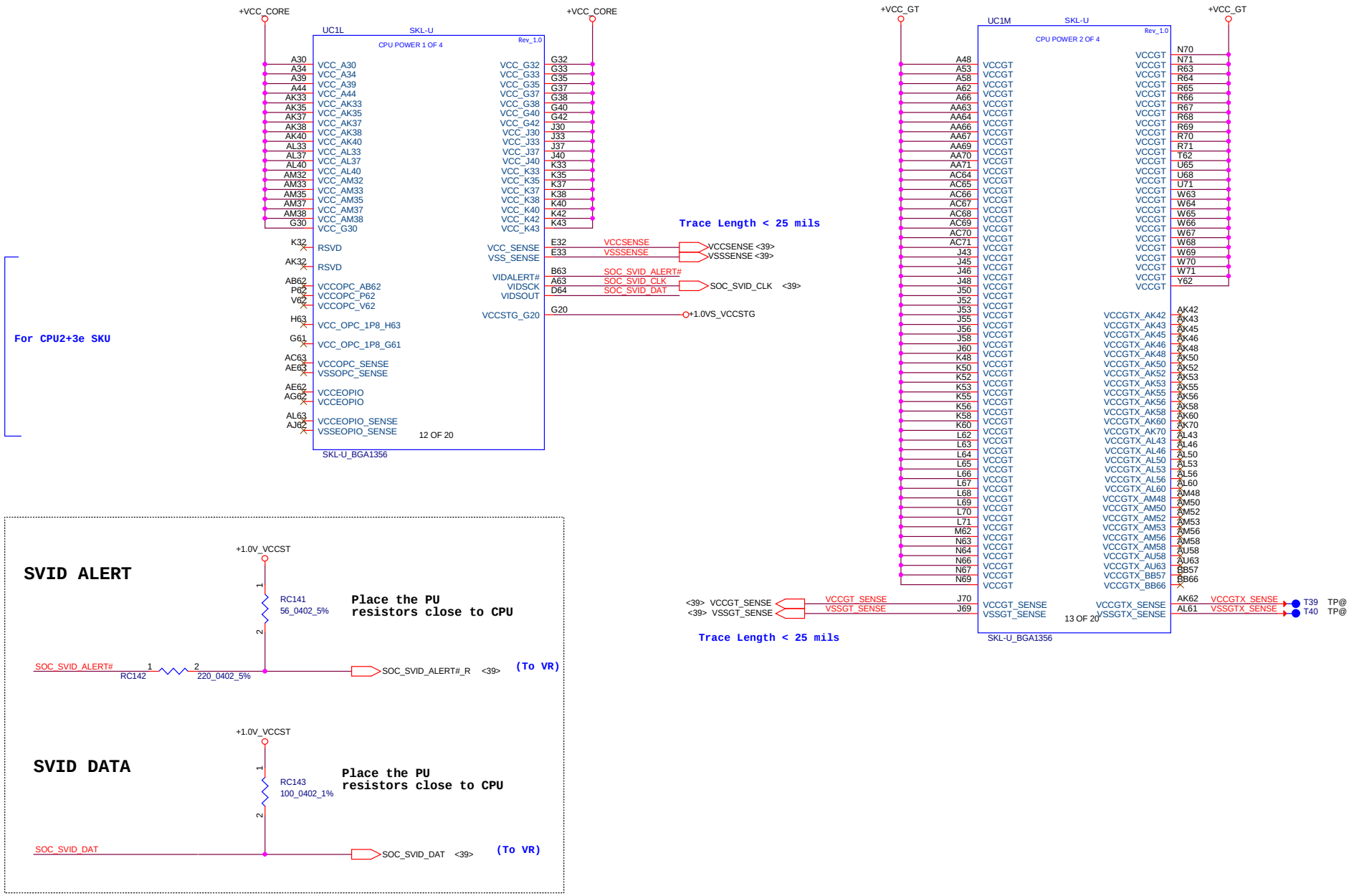

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Compal Electronics, Inc.

Title	SKL-U(10/12)POWER,SVID
Size	Document Number: B3ZMS LA-D591P
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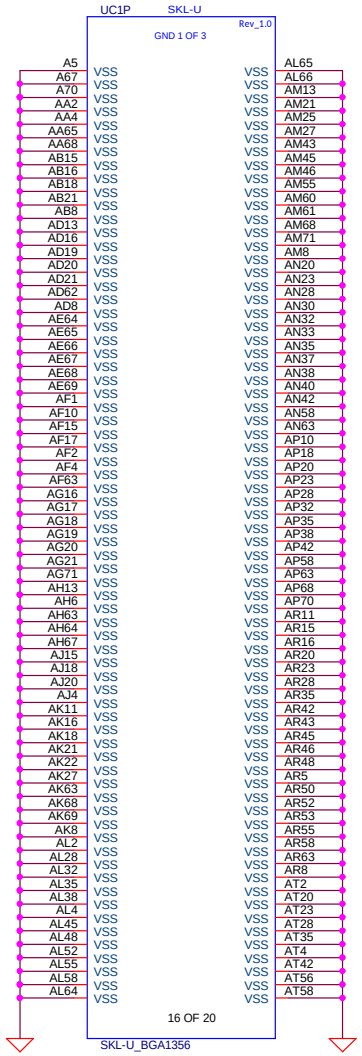

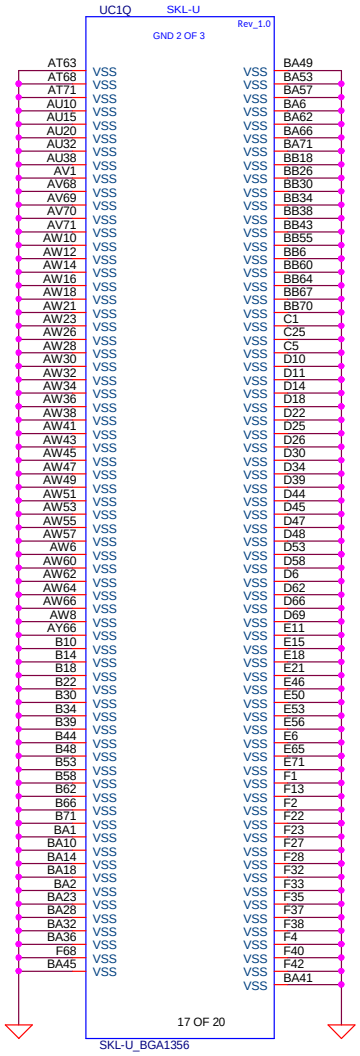

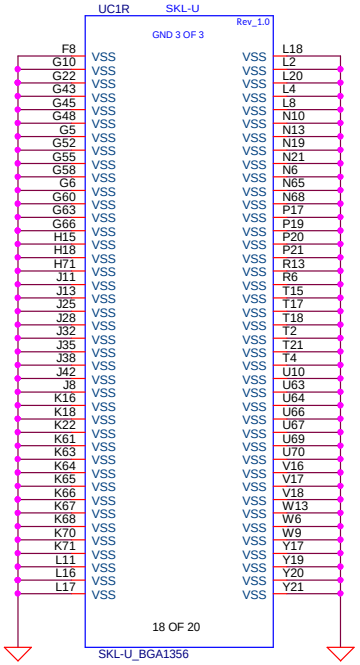

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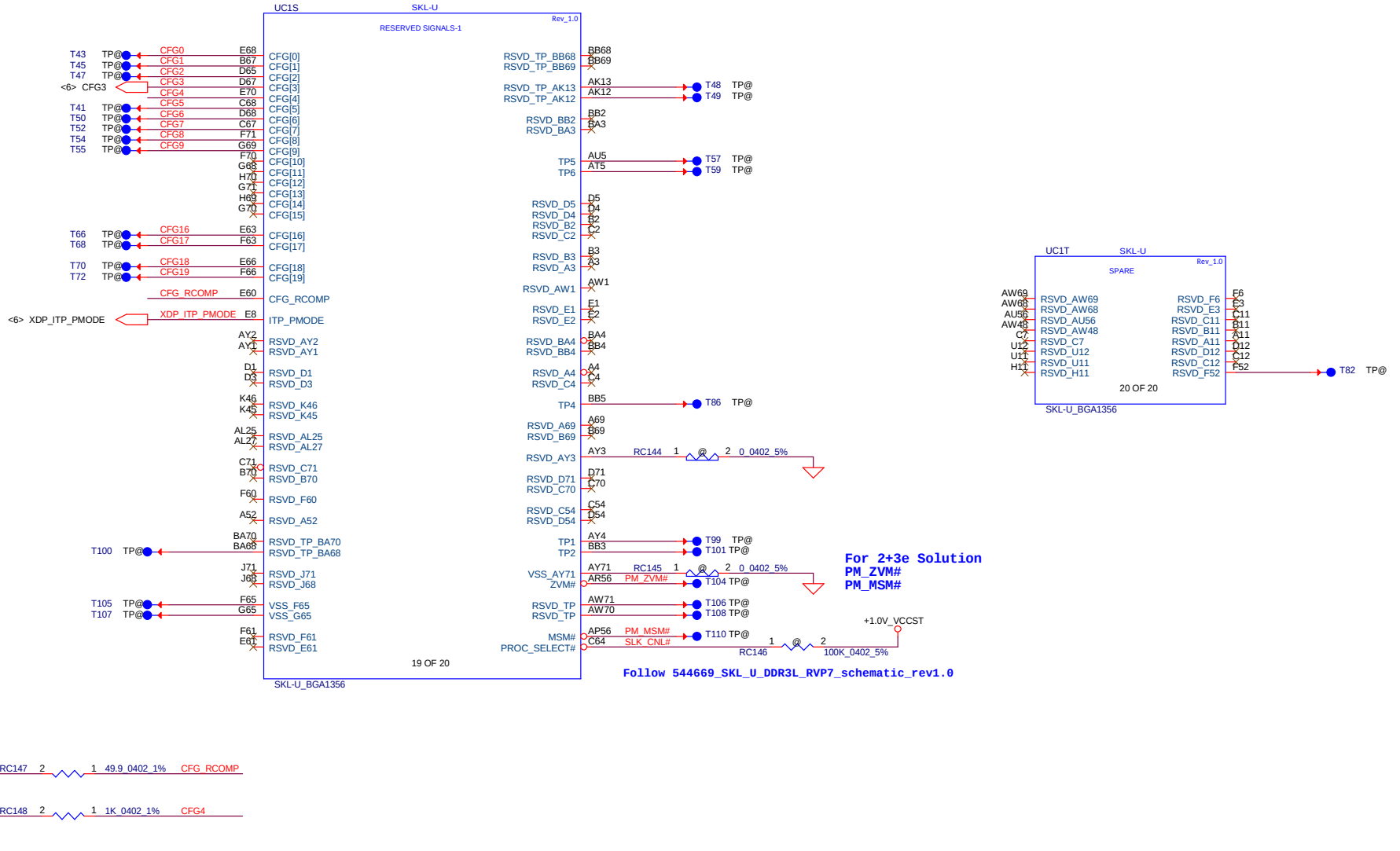
Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size | Document Number: B3ZMS LA-D591P | Rev: 2.0

Date: Wednesday, February 24, 2016 | Sheet 16 of 45



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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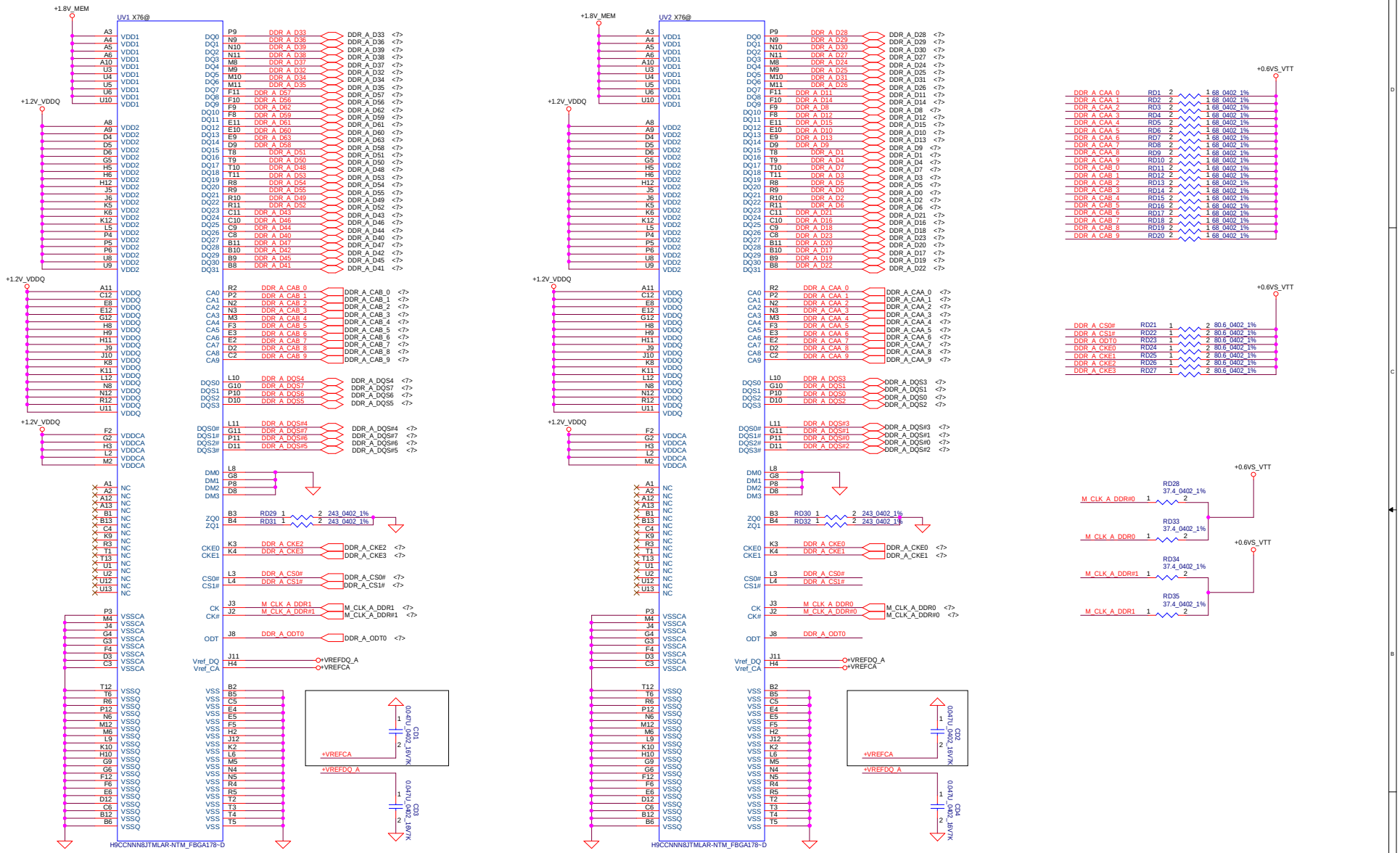
Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size	Document Number	Rev
	B3ZMS LA-D591P	2.0

Date: Wednesday, February 24, 2016 Sheet 17 of 45



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Compal Electronics, Inc.

Title: **LPDDR3 A**

Size	Document Number	Rev
C	B3ZMS LA-D591P	2.0

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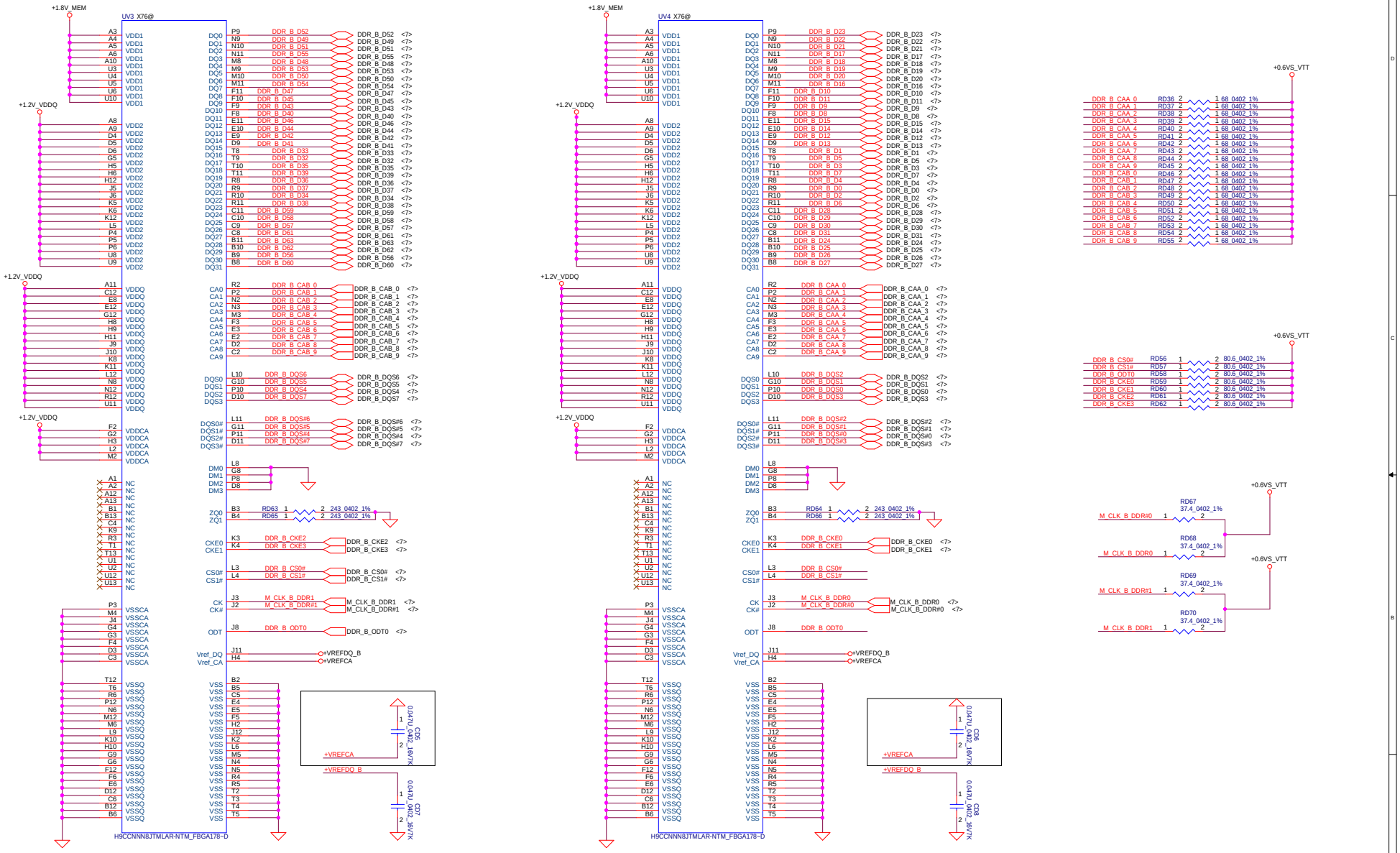

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Title: **LPDDR3_B**

Size	Document Number	Rev
	B3ZMS LA-D591P	2.0

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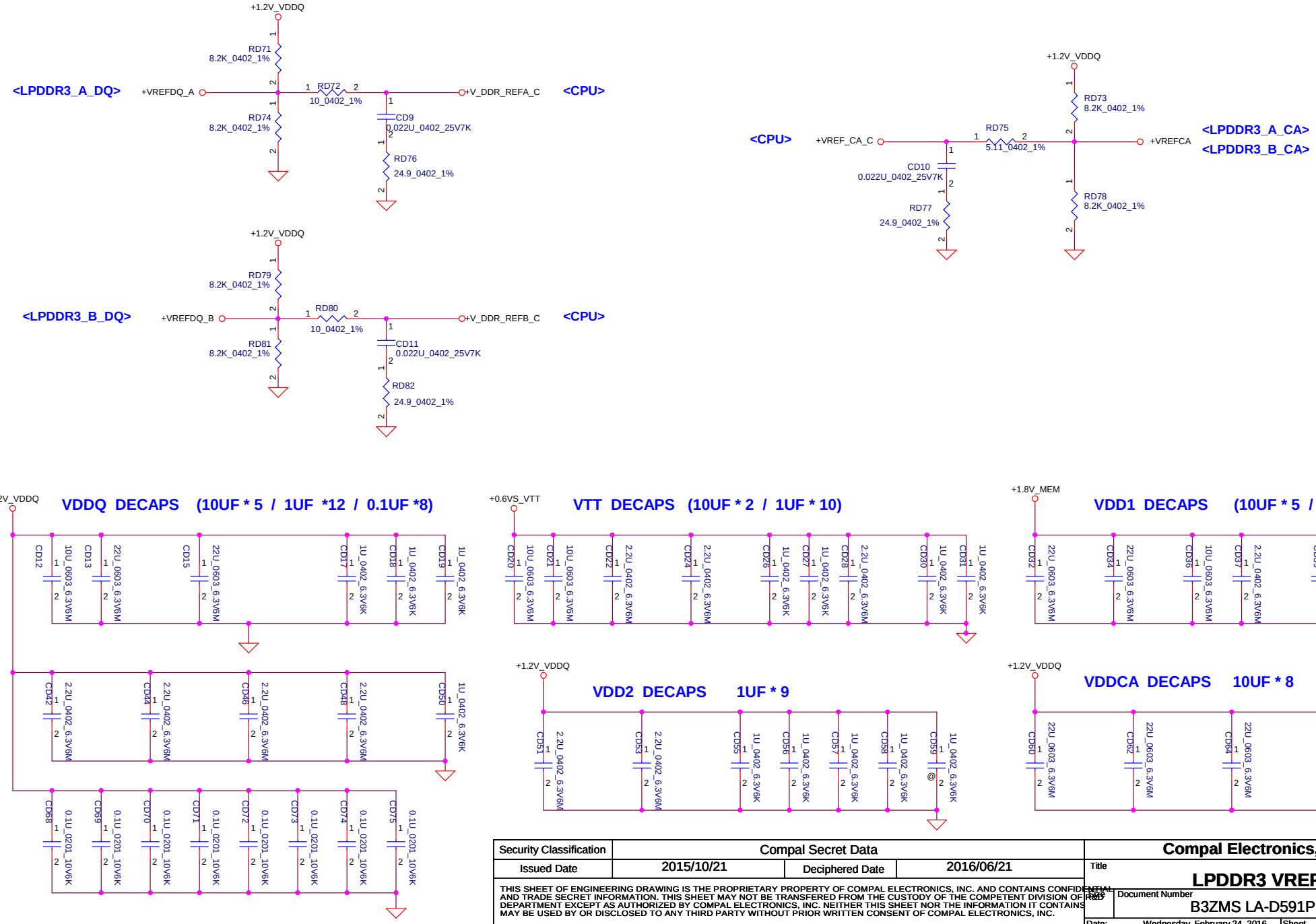

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Compal Electronics, Inc.

Title: **LPDDR3 VREF**

Document Number: B3ZMS LA-D591P

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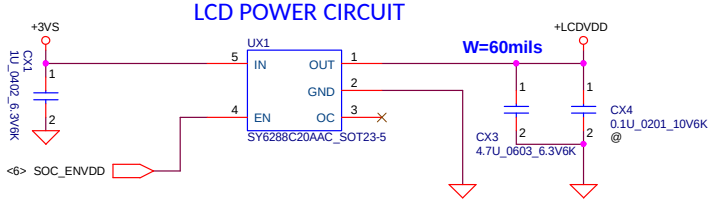
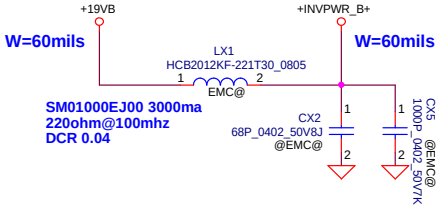
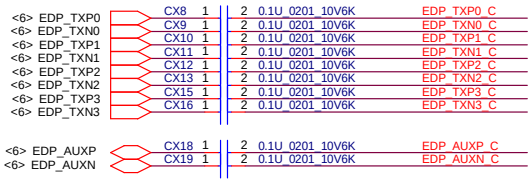
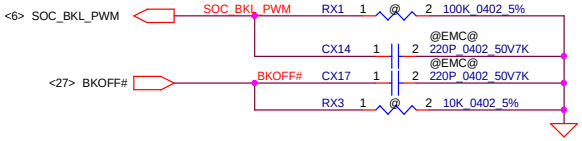
LCD POWER CIRCUIT

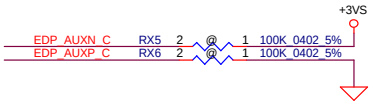


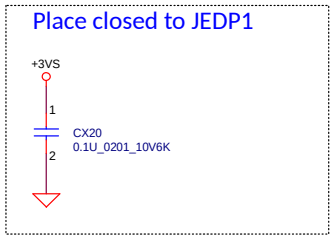


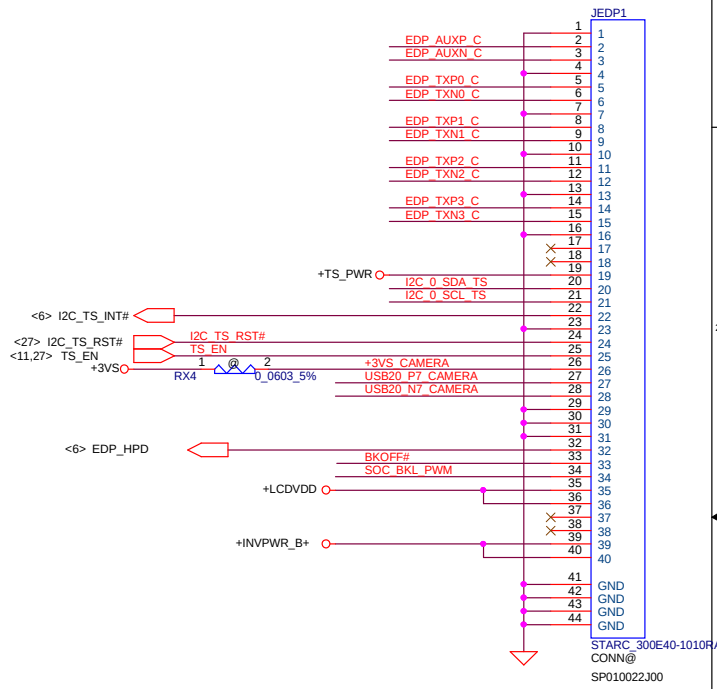
LCD/LED PANEL Conn.



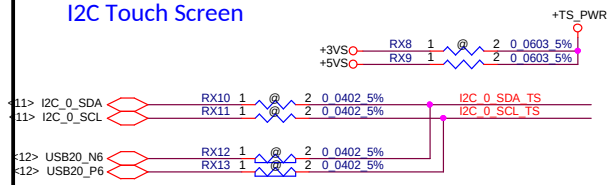




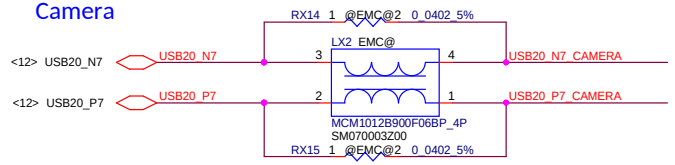




I2C Touch Screen



Camera



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Issued Date	2015/10/21	Deciphered Date	2016/06/21

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Compal Electronics, Inc.

Title: **eDP Connector**

Size	Document Number	Rev
Custom	B3ZMS LA-D591P	2.0

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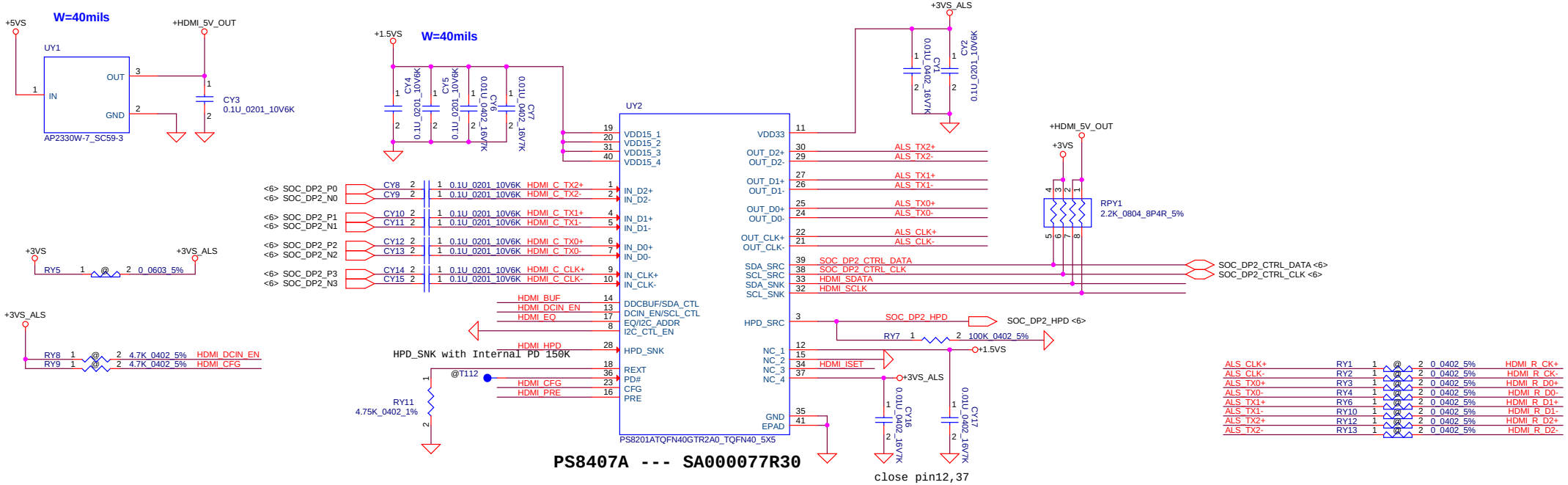

Security Classification	Compal Secret Data		
Issued Date	2015/10/21	Deciphered Date	2016/06/21

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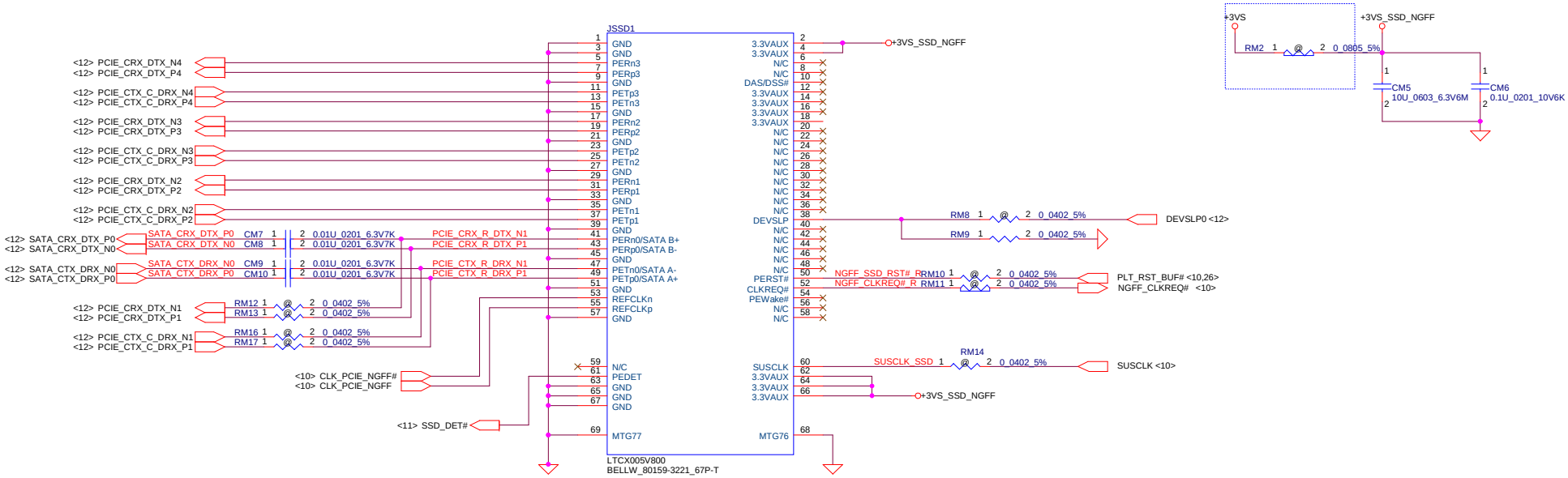
Compal Electronics, Inc.	
Title	HDMI CONN.
Size: Custom	Document Number: B3ZMS LA-D591P
Rev	2.0
Date: Wednesday, February 24, 2016	Sheet 22 of 45



Security Classification	Compal Secret Data		
Issued Date	2015/10/21	Deciphered Date	2016/06/21

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Compal Electronics, Inc.

Title: **mSATA & NFC**

Size: Custom | Document Number: **B3ZMS LA-D591P** | Rev: 2.0

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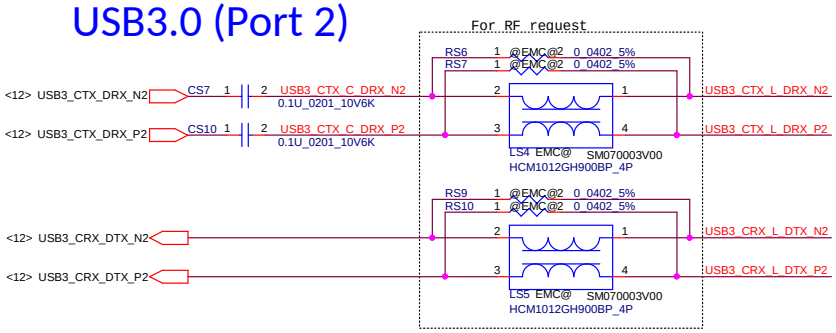
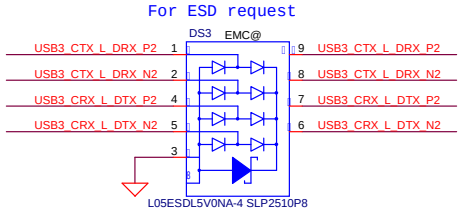
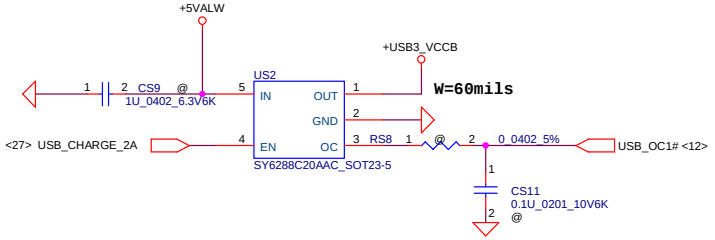
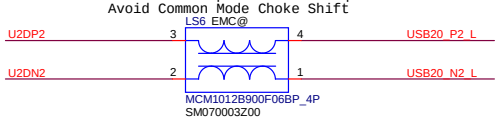
USB3.0 (Port 2)

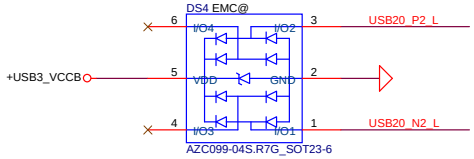


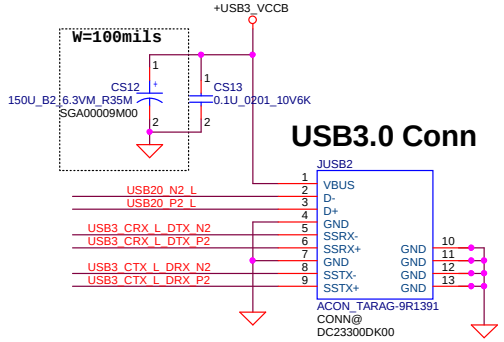




Note: (A4WAS PVT)
Delete 0 ohm path for DFX request
Avoid Common Mode Choke Shift

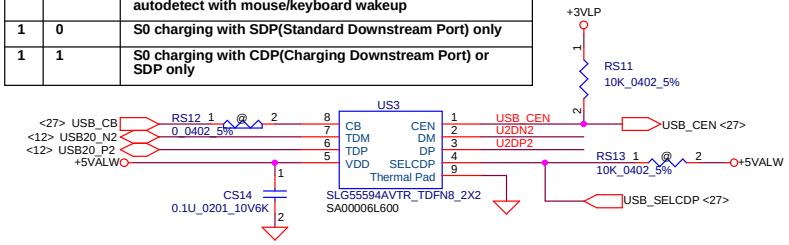






USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



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Compal Electronics, Inc.

Title: **USB3.0 Conn/USB_B**

Size: Custom | Document Number: **B3ZMS LA-D591P** | Rev: 2.0

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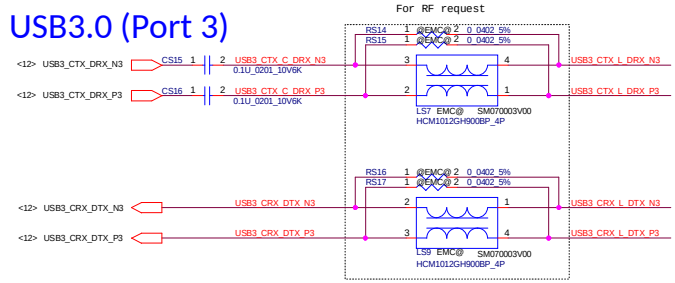

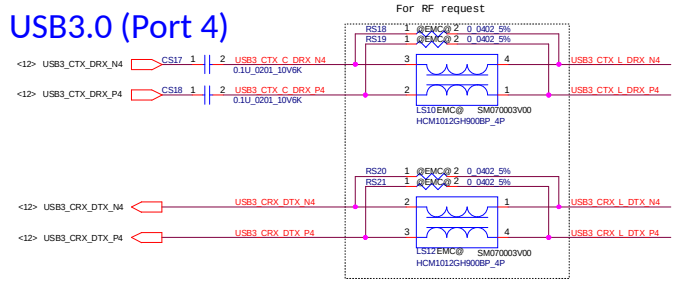

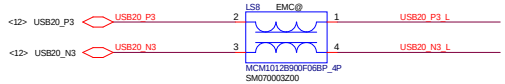

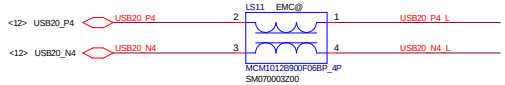

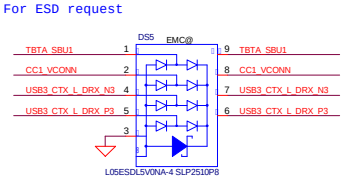

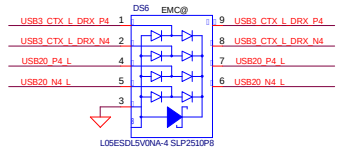

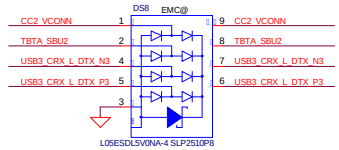

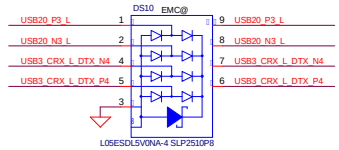

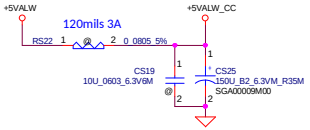

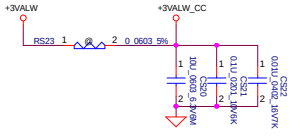

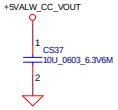

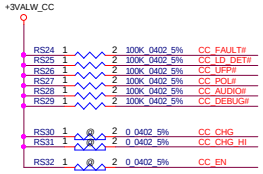

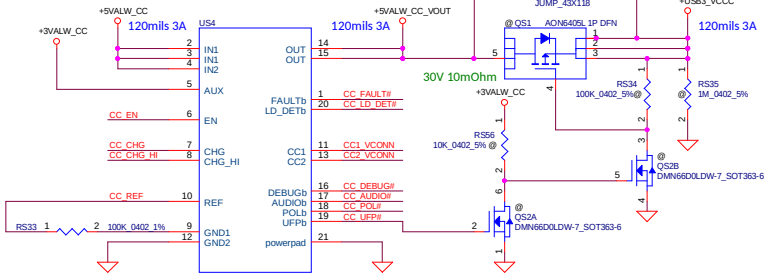

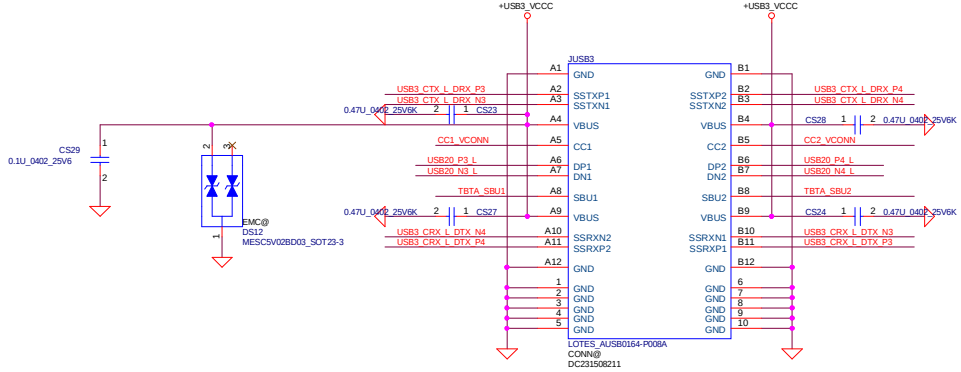

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Issued Date	2015/10/21	Deciphered Date	2016/06/21

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Compal Electronics, Inc.

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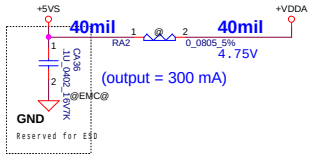
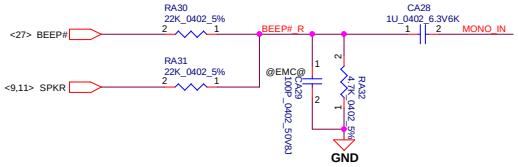
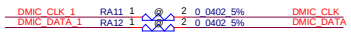
Audio

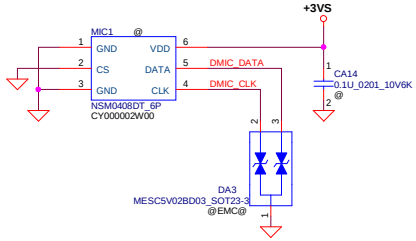




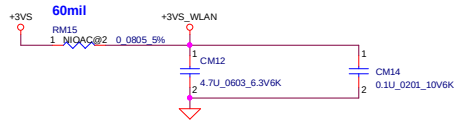
Digital MIC Singal-MIC

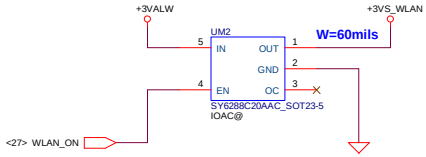
MIC BOM upload by Audio Team





Wireless LAN





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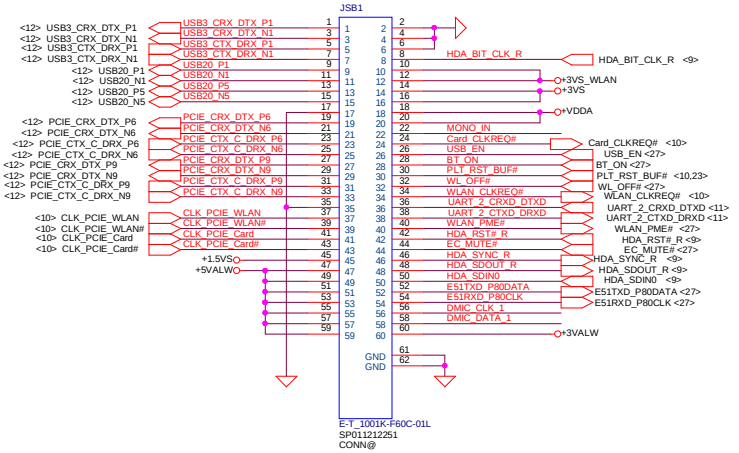

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Compal Electronics, Inc.

Title: *P29-CardRead/RTS5229*

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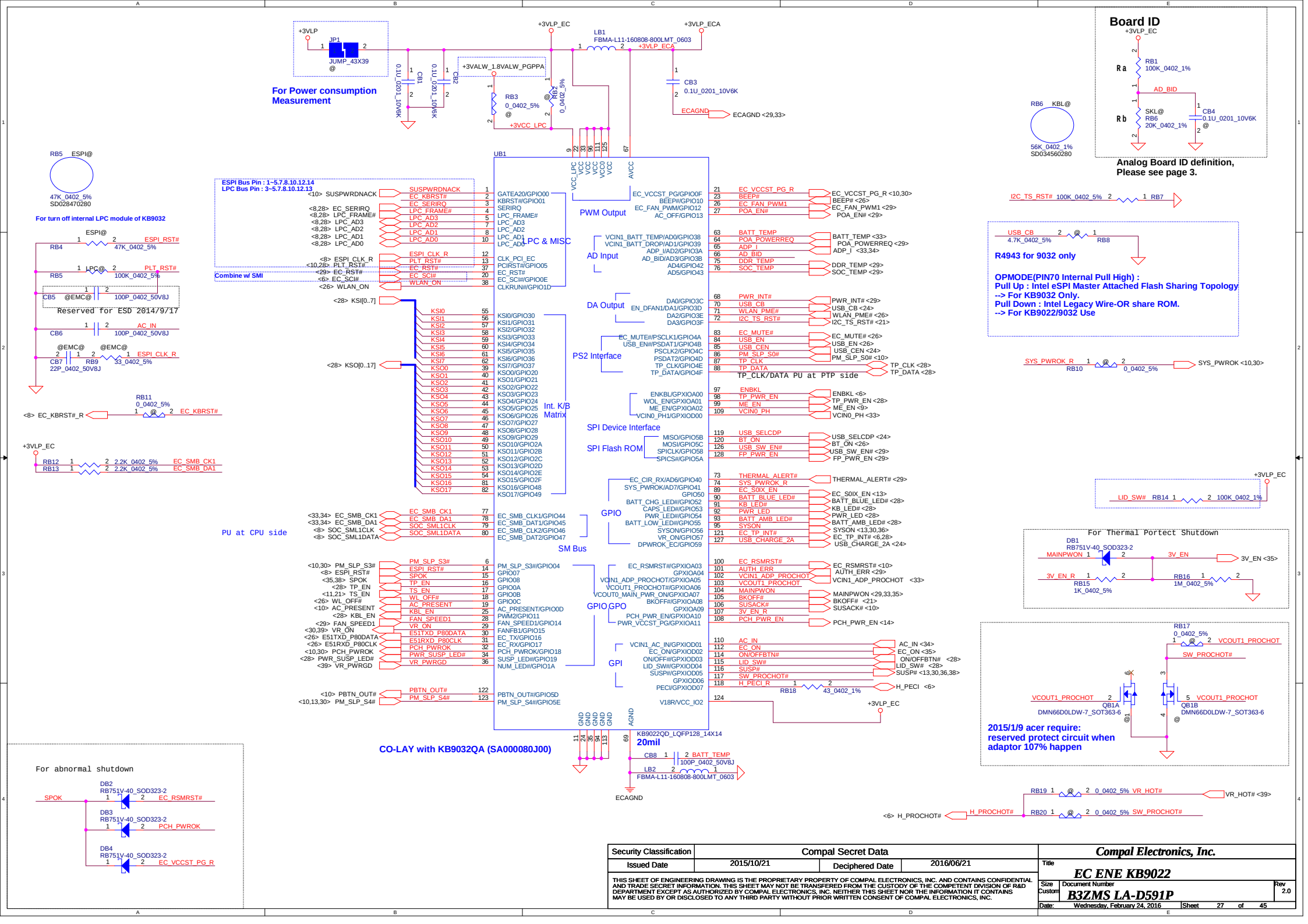

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Compal Electronics, Inc.

Title: EC ENE KB9022

Size: Custom | Document Number: B3ZMS LA-D591P | Rev: 2.0

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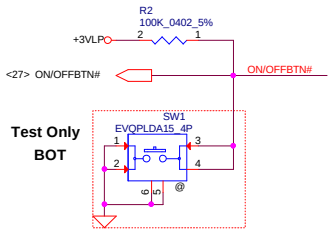
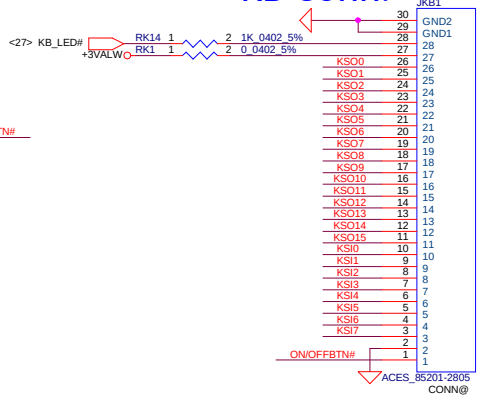
KB Conn.

ON/OFF BTN





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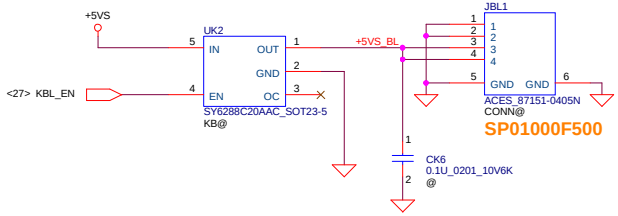
KB BackLight Conn. Reserve



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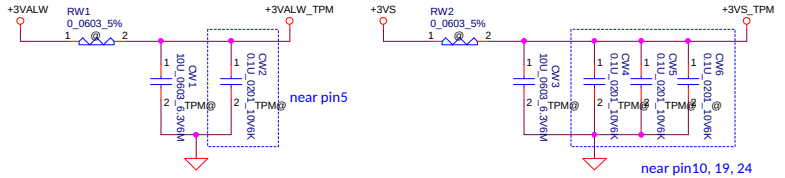
TPM Board for 2015



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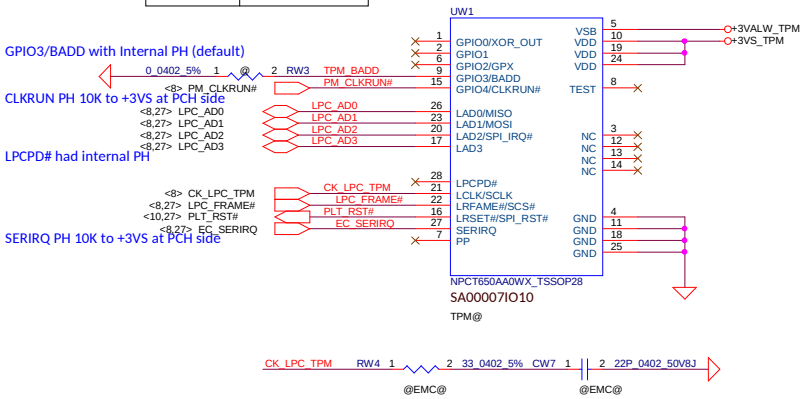
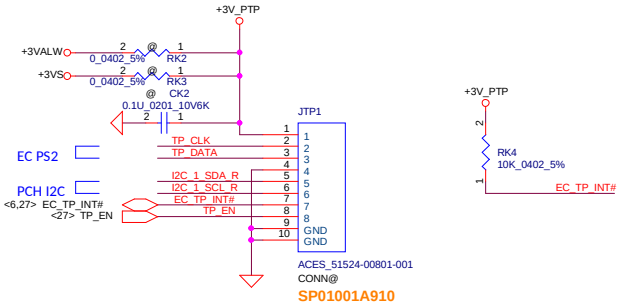
0	EEh - EFh
* 1	7Eh - 7Fh



TP/B Conn.



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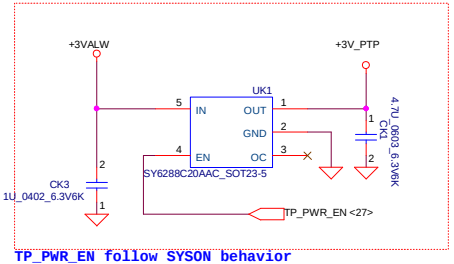
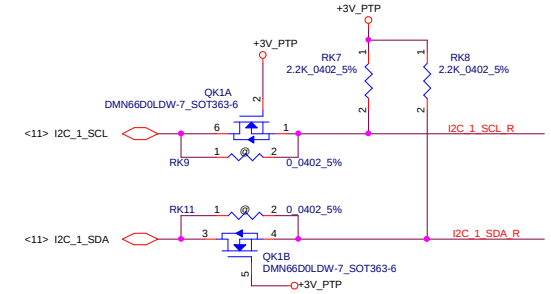
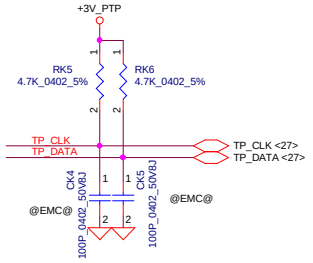
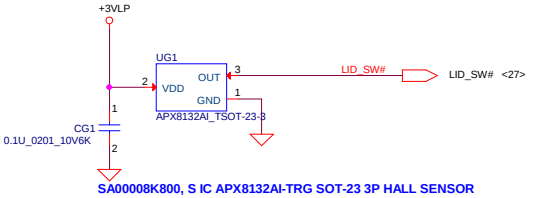






Lid Switch

(Hall Effect Switch)



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

LED

Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

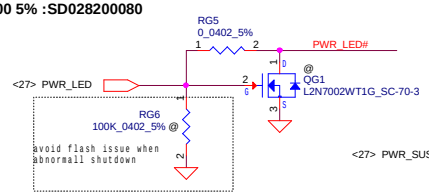
Vf @ 5 mA :

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

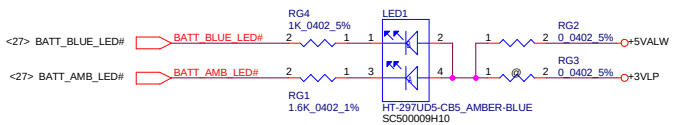
CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080

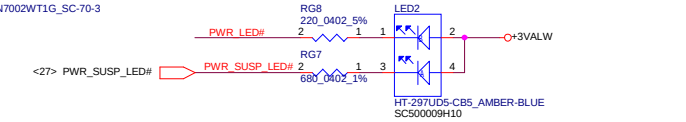
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080



Battery LED



Power LED



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Compal Electronics, Inc.

Title: KB & TP & TPM Connector & LED

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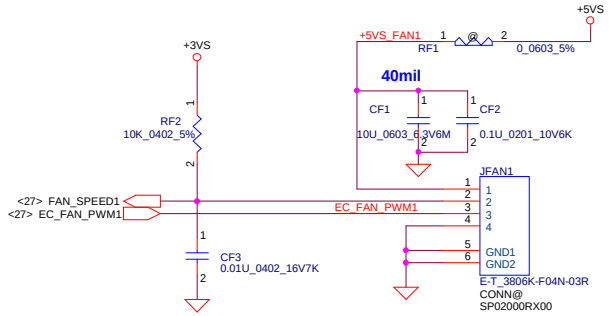
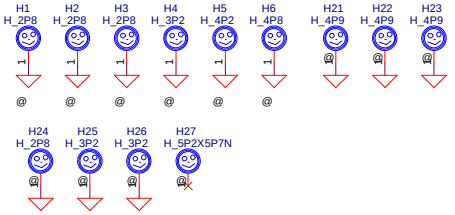
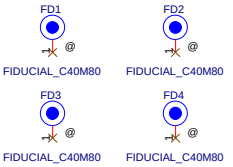
FAN

FAN Conn1

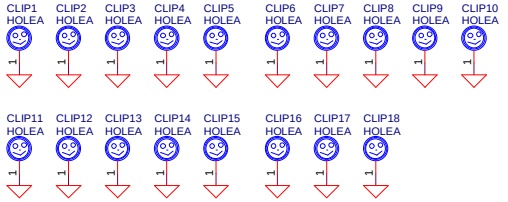


Screw Hole

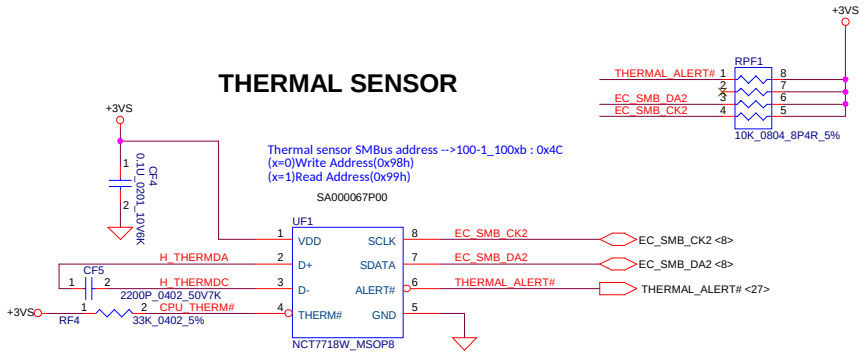




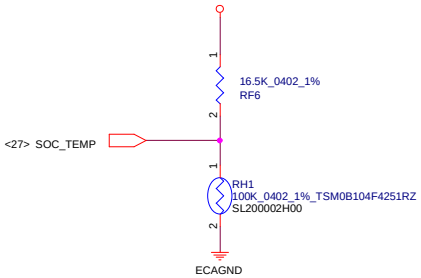
CLIP



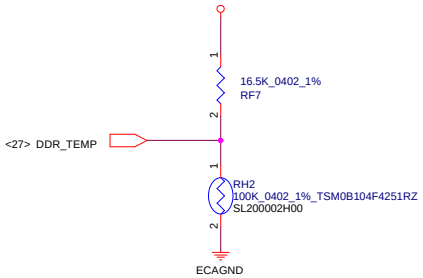
THERMAL SENSOR



Close to SOC

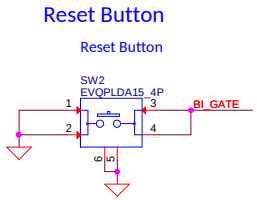


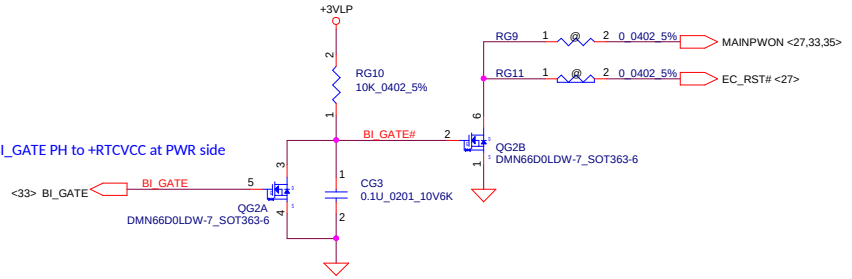
Close to DDR



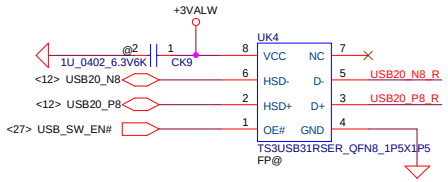
Reset Circuit

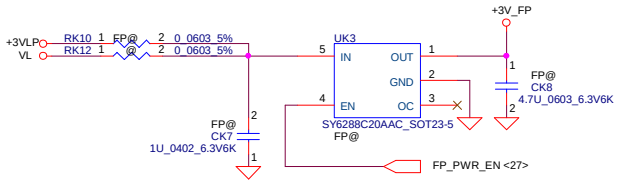
Reset Button

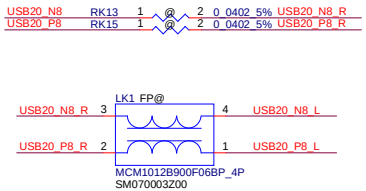


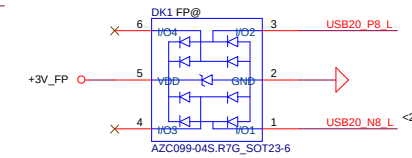


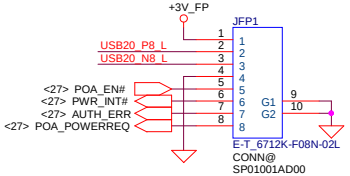
Finger Print











Finger Print GPIO table

Signal Name	Active H/L	Direction	Description
POA_EN#	Low	Host to FPR	to activate the POA functionality
POA_POWERREQ	High	FPR to Host	To request additional power while acquiring/matching fingerprint
PWR_INT#	Low	FPR to Host	trigger power on event to EC
Auth_ERR	High	FPR to Host	to notify EC to error pattern LED or message
USB_SW_EN	High		Enable USB LS SW
FP_PWREN	High		control FP switch power enable

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Compal Electronics, Inc.

Title: FAN & Screw Hole & G-Sensor

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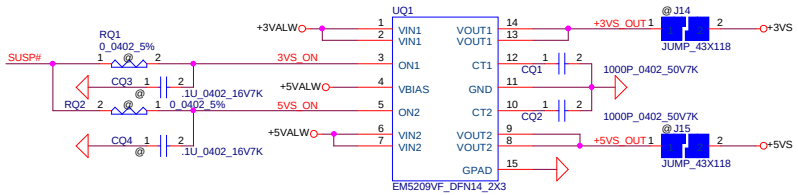
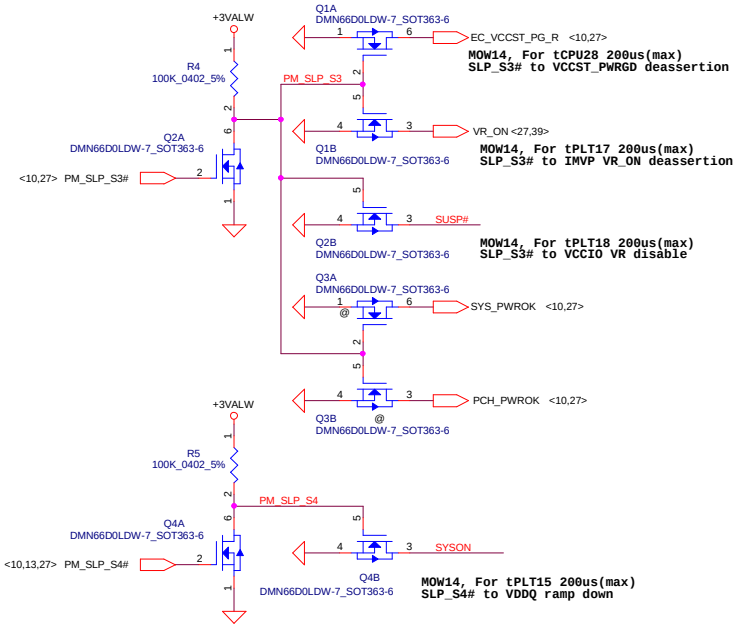
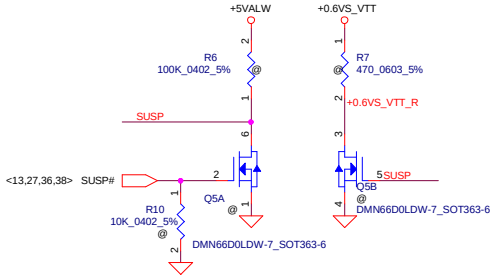
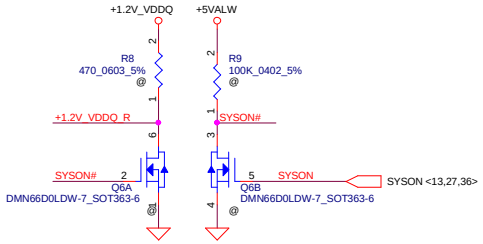
DC Interface



For Power ON/Off Sequence







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Compal Electronics, Inc.

Title: **DC Interface**

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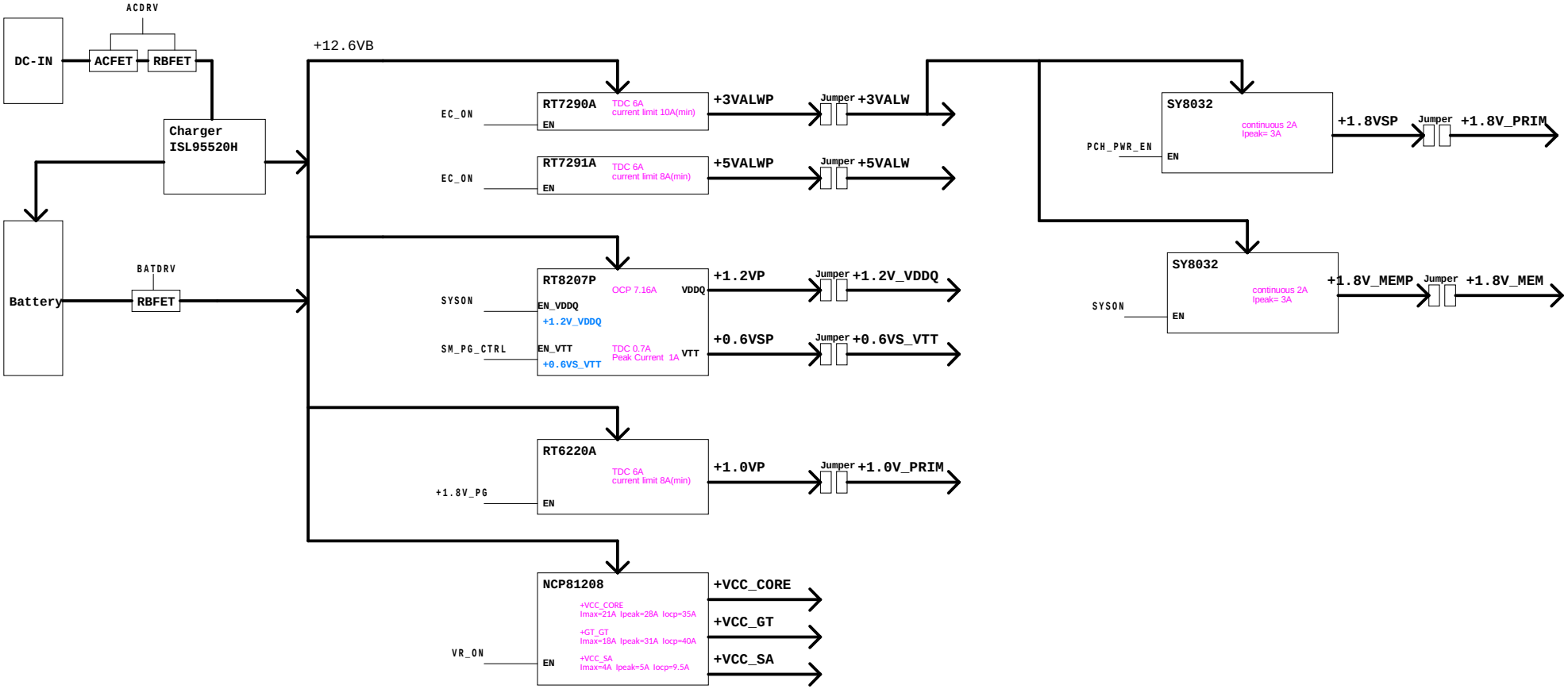

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Compal Electronics, Inc.

Title	Power Block Diagram	
Size	Document Number: B3ZMS LA-D591P	Rev: 2.0
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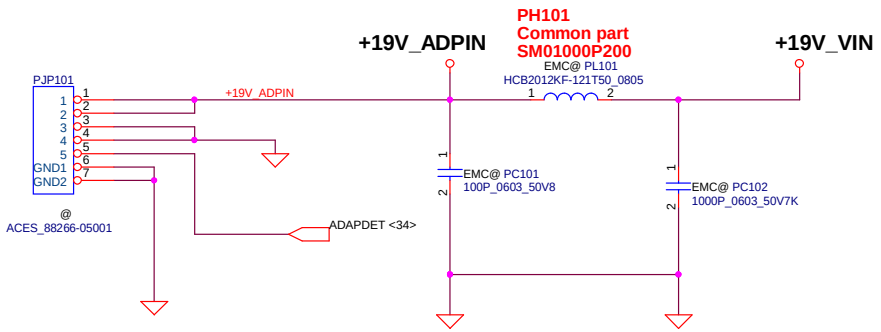

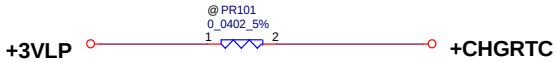

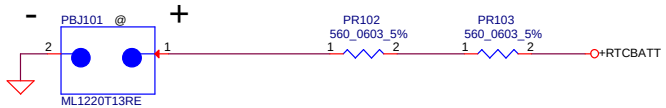

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Title	DC Conn	
Size	Document Number: LA-C482P	Rev: 2.0
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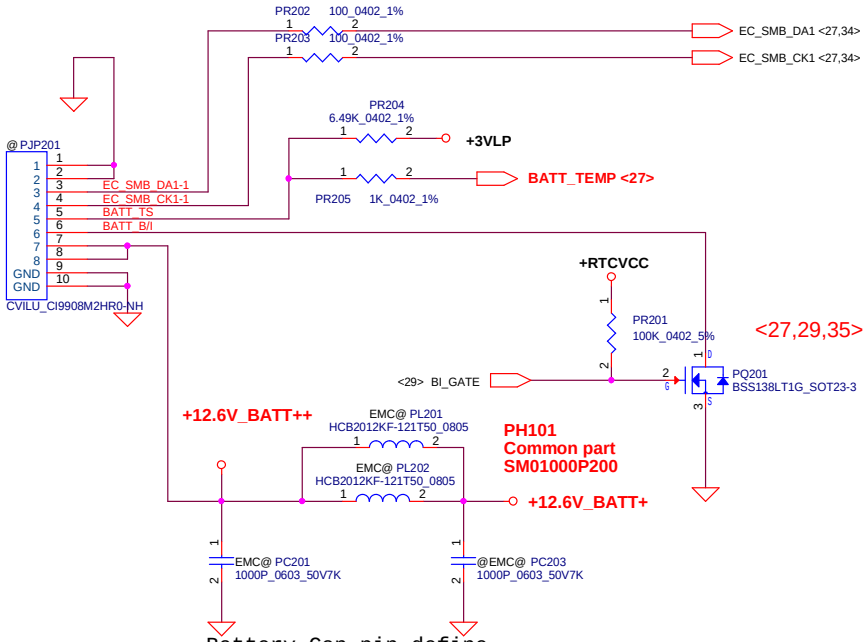
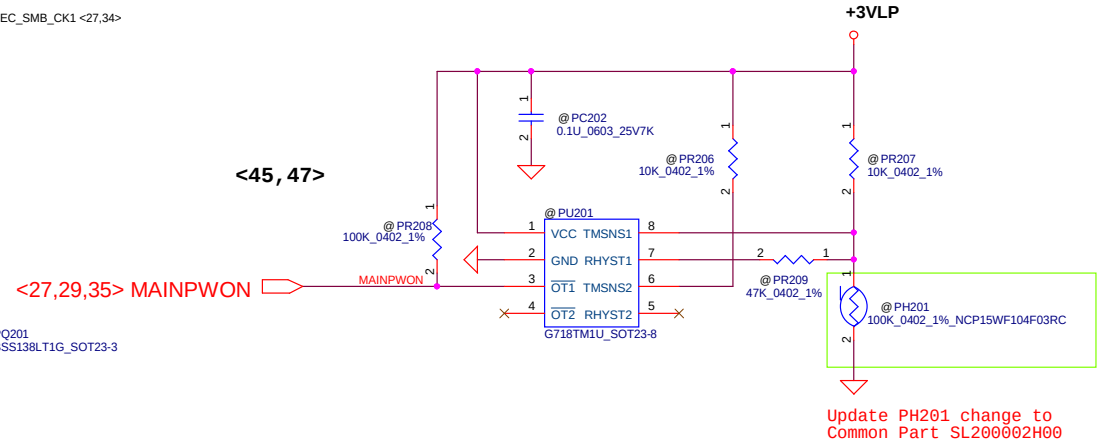




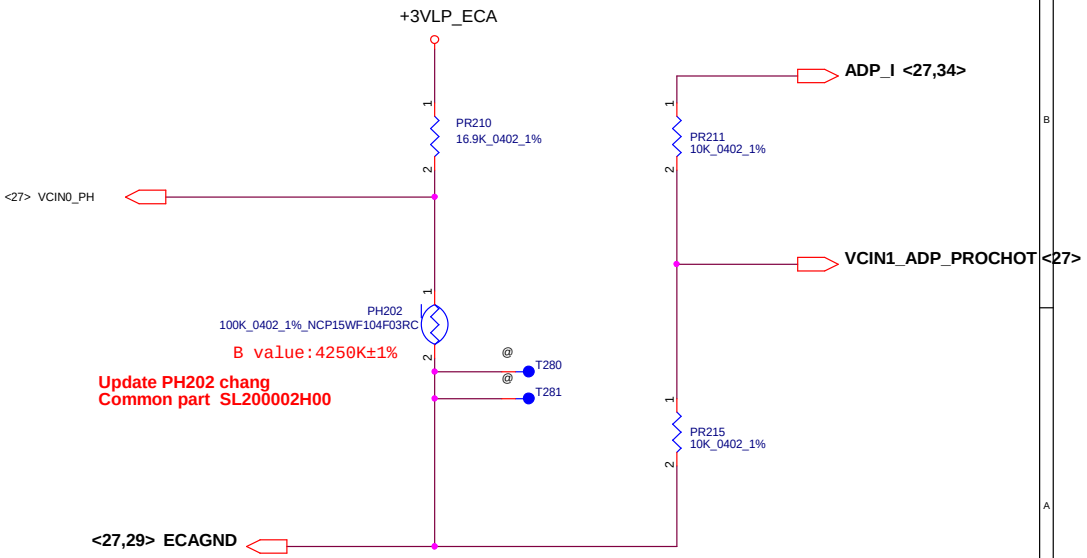

```
---Battery_pin define---
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7  Batt+
PIN8  Batt+
```

```
---Battery Con_pin define---
PIN8   GND
PIN7   GND
PIN6   SMD
PIN5   SMC
PIN4   TS
PIN3   B/I
PIN2   Batt+
PIN1   Batt+
```

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.V
PH202(ohm)	7.3K	26.11K

For KB9022 sense 20mΩ	Active	Recovery
45W PR211=10K ohm	0.61V(58.5W)	0.47V(45W)

PH202 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C



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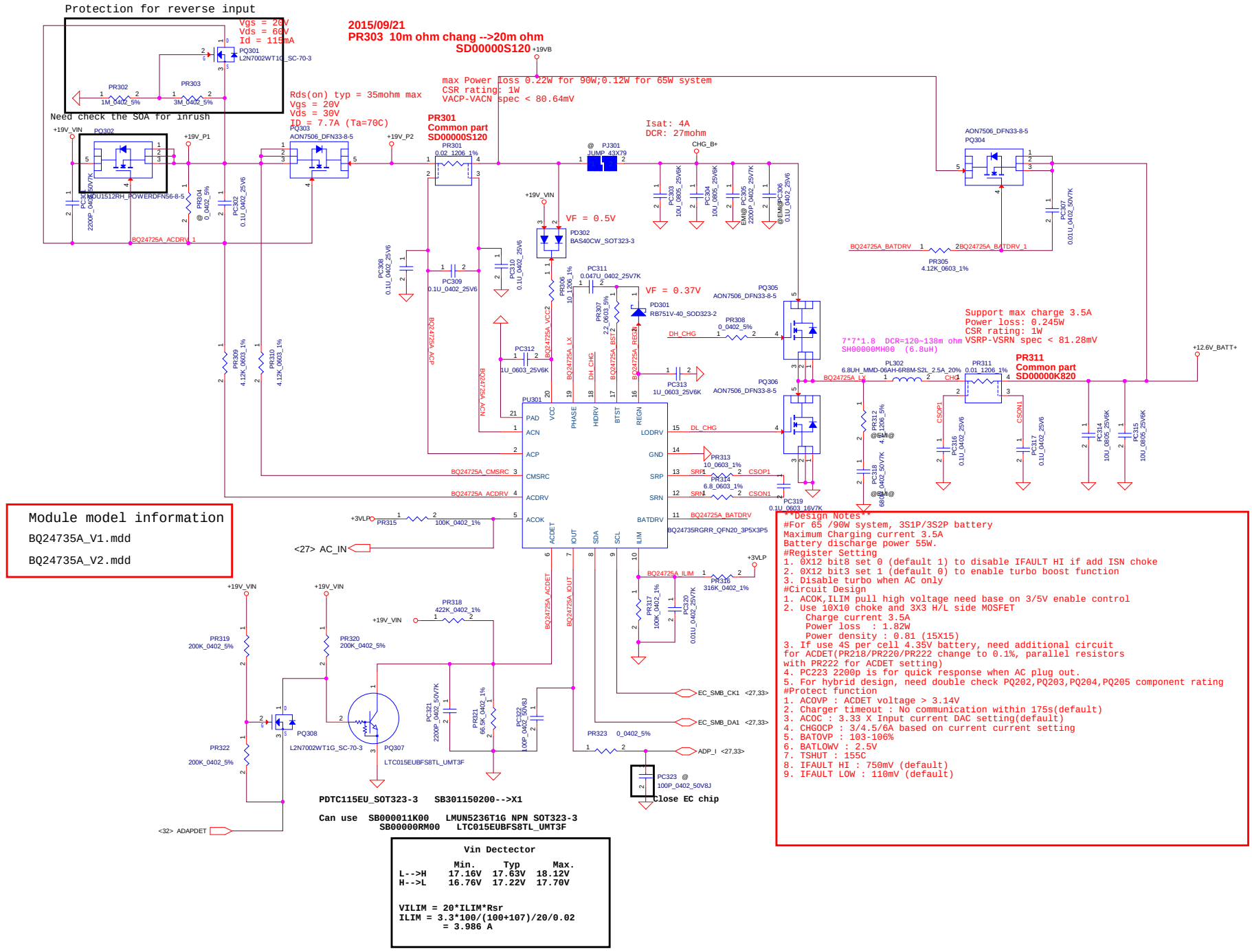
Title	BATT Conn		
Size	Document Number: LA-C482P		Rev: 2.0
Date:	Wednesday, February 24, 2016	Sheet 33 of 43	



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Issued Date	2015/1/15	Deciphered Date 2017/10/09	Title: CHARGER

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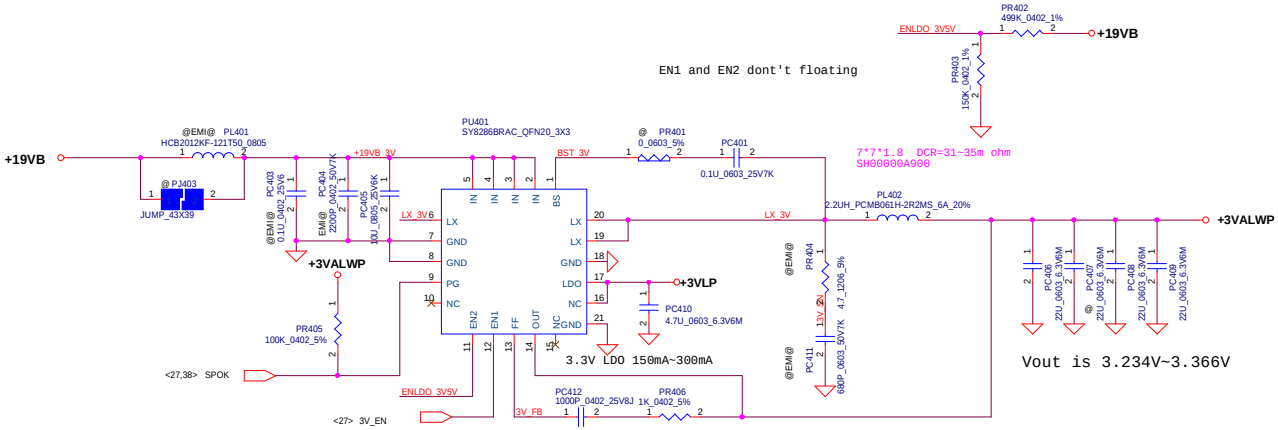
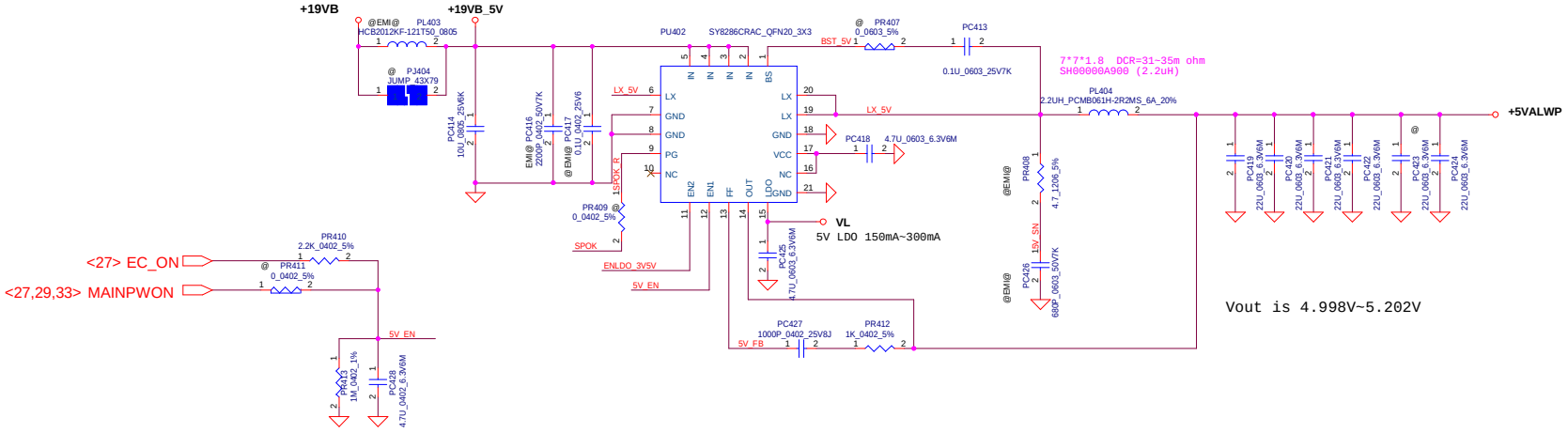
Size: Custom	Document Number: LA-C482P		Rev: 2.0
Date:		Sheet 34 of 43	





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Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size	Document Number	Rev
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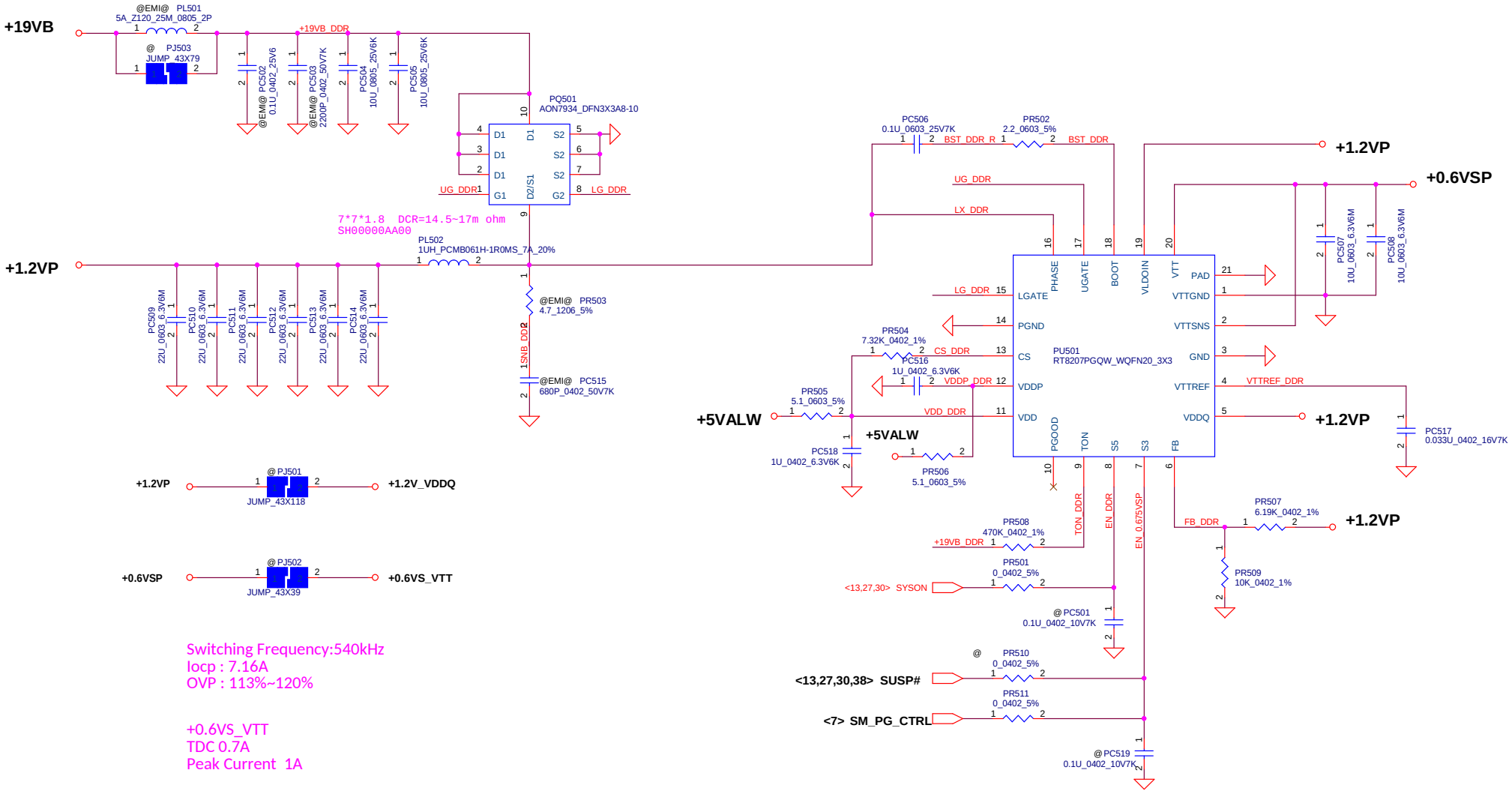

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Issued Date	2015/1/15	Deciphered Date	2017/10/09

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Title: **1.2V/0.6VS**

Size	Document Number	Rev
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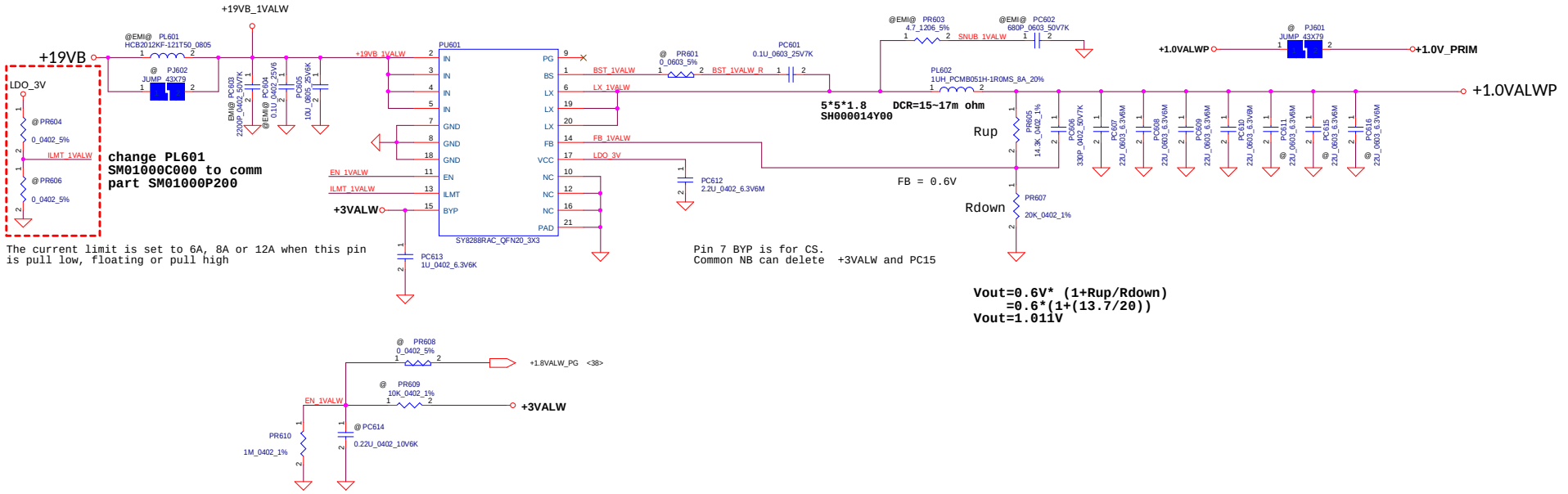
Module model information

SYX196D_V3.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(13.7/20))
Vout=1.011V

Security Classification	Compal Secret Data		
Issued Date	2015/1/15	Deciphered Date	2017/10/09

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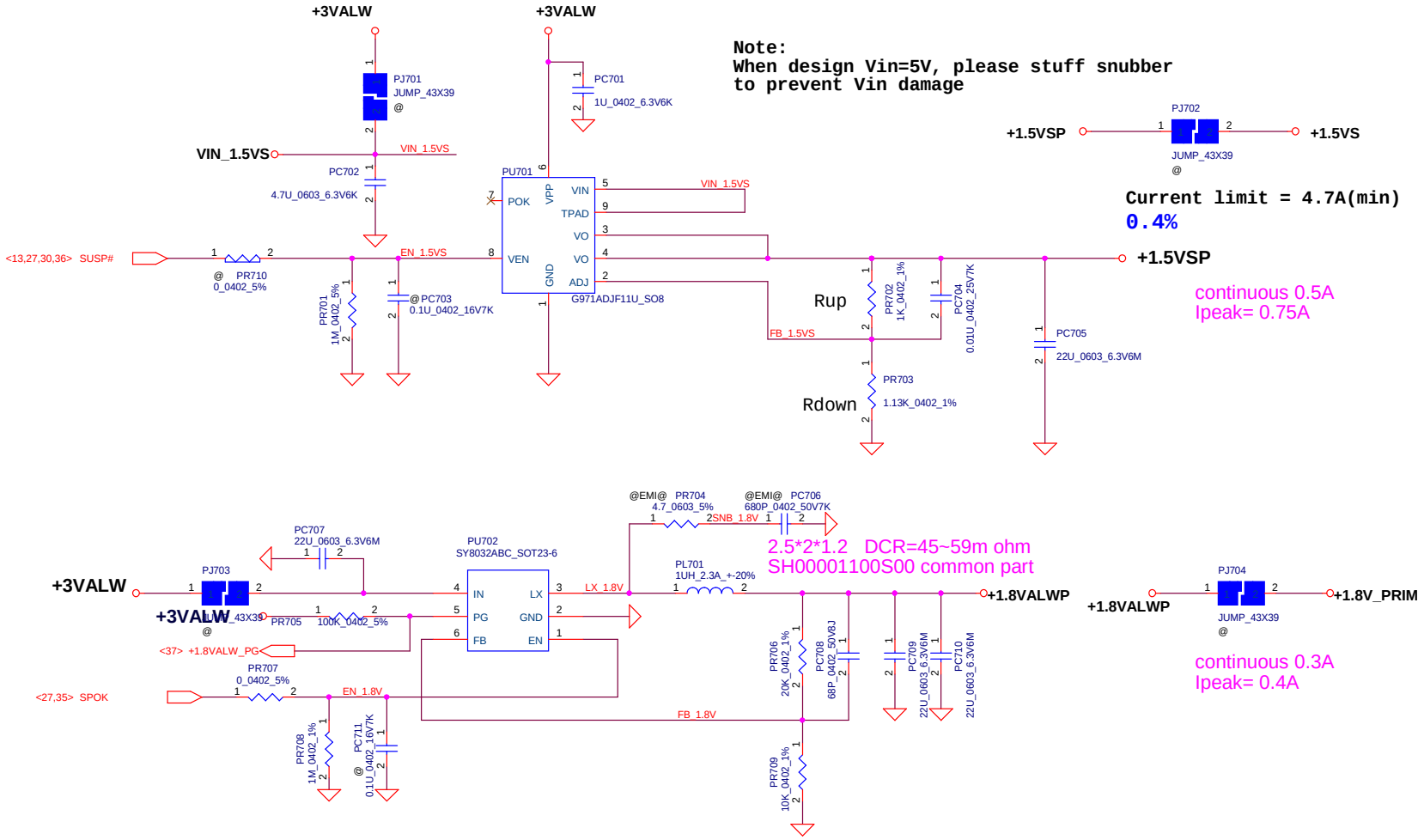
Compal Electronics, Inc.

Title	1.0V_PRIM	
Size	Document Number: LA-C482P	Rev: 2.0
Date: Wednesday, February 24, 2016	Sheet 37 of 43	



Security Classification	Compal Secret Data		
Issued Date	2015/1/15	Deciphered Date	2017/10/09

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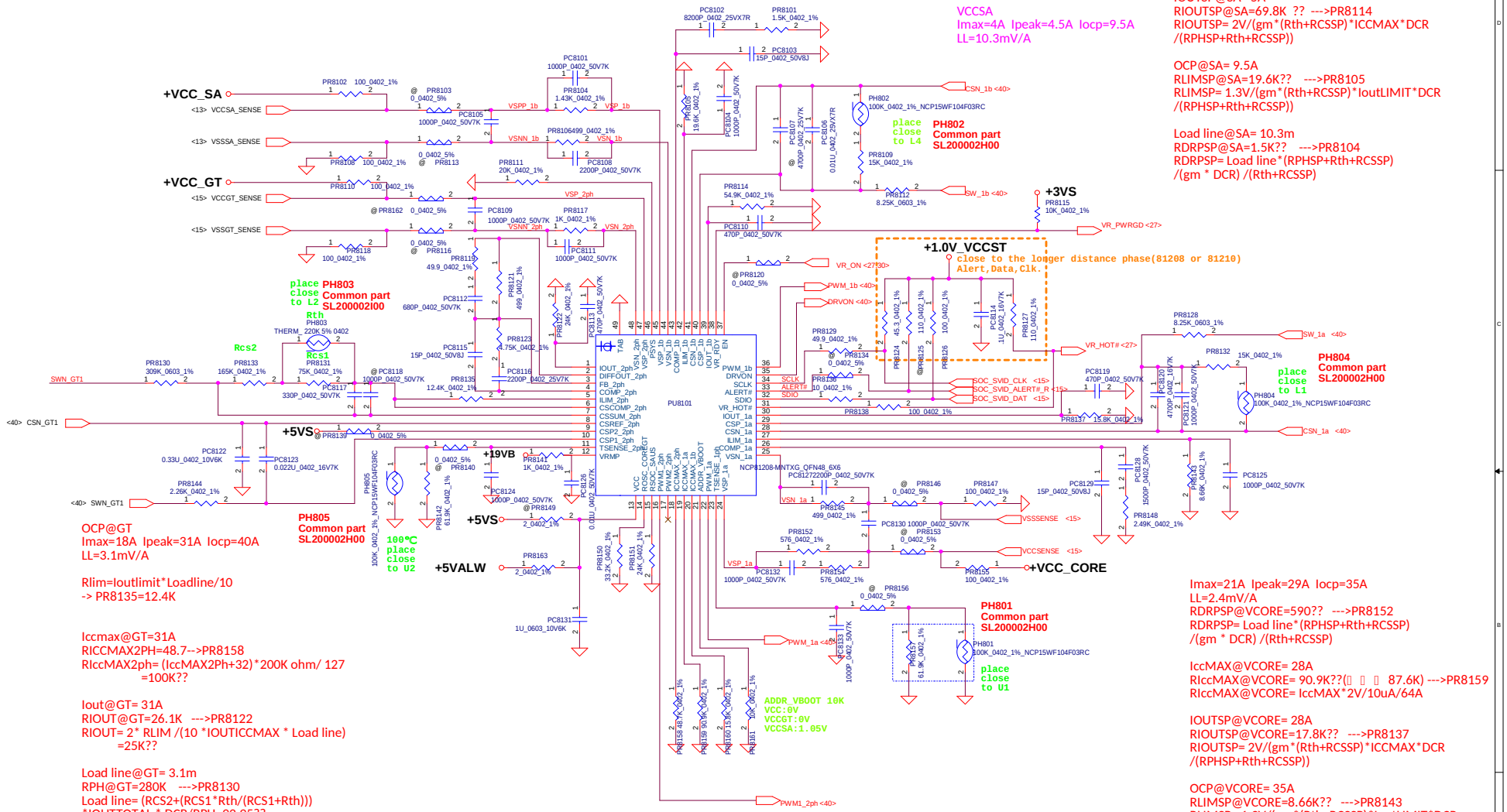
Compal Electronics, Inc.

Title	1.8V_PRIM / 1.8V_MEM	
Size	Document Number: LA-C482P	Rev: 2.0
Date: Wednesday, February 24, 2016	Sheet 38 of 43	



VCORE
Imax=21A Ipeak=29A Iocp=35A
LL=2.4mV/A

GT
Imax=18A Ipeak=31A Iocp=40A
LL=3.1mV/A

VCCSA
Imax=4A Ipeak=4.5A Iocp=9.5A
LL=10.3mV/A

Imax=4A Ipeak=4.5A Iocp=9.5A
LL=10.3mV/A
IccMAX@SA= 5A

RIccMAX@SA= 15.8K --->
RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ?? --->
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=19.6K?? --->
RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.5K?? --->
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

OCP@GT
Imax=18A Ipeak=31A Iocp=40A
LL=3.1mV/A

Rlim=Ioutlimit*Loadline/10
-> PR8135=12.4K

Iccmax@GT=31A
RICCMAX2PH=48.7-->
RIccMAX2ph= (IccMAX2Ph+32)*200K ohm/ 127
=100K??

Iout@GT= 31A
RIOUT@GT=26.1K --->
RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)
=25K??

Load line@GT= 3.1m
RPH@GT=280K --->
Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH=92.95??

Imax=21A Ipeak=29A Iocp=35A
LL=2.4mV/A
RDRPSP@VCORE=590?? --->
RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RIccMAX@VCORE= 90.9K??(87.6K) -->
RIccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=17.8K?? --->
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=8.66K?? --->
RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Security Classification	Compal Secret Data		
Issued Date	2015/1/15	Deciphered Date	2017/10/09

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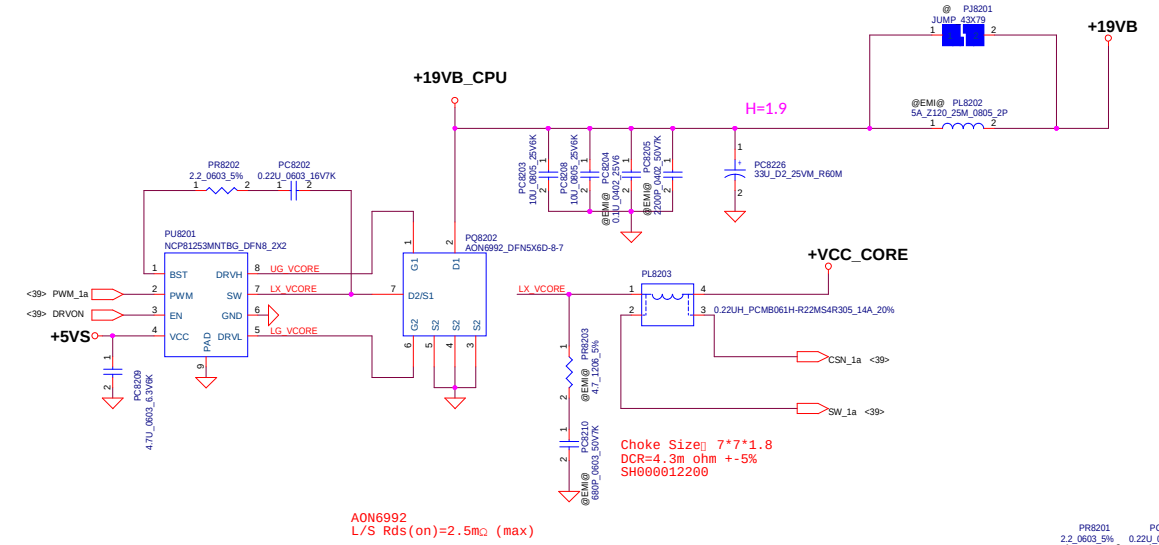
Compal Electronics, Inc.

Title: **CPU Power rail**

Size	Document Number	Rev
	LA-C482P	2.0

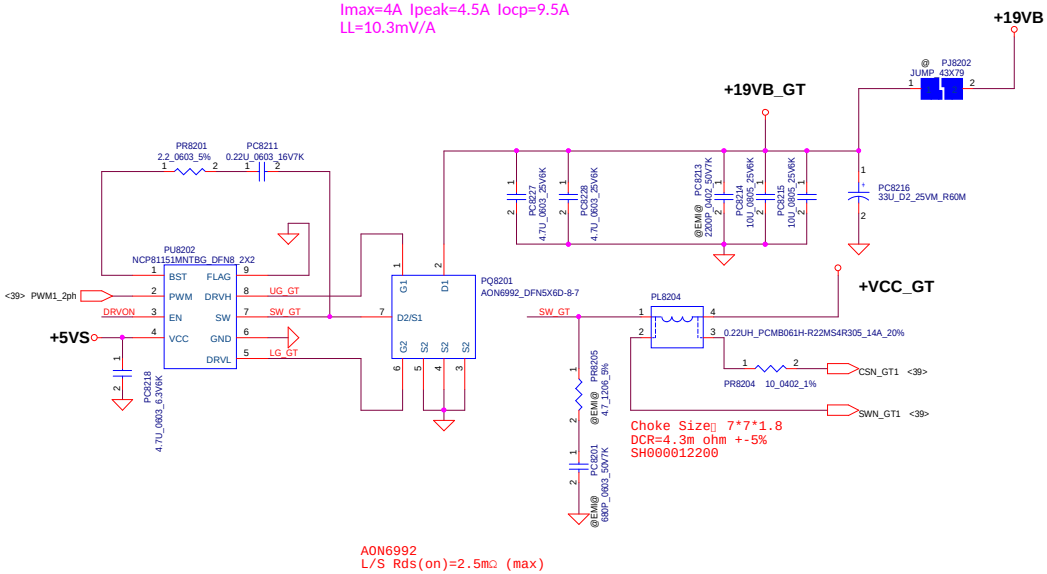
Date: Wednesday, February 24, 2016 Sheet 39 of 43

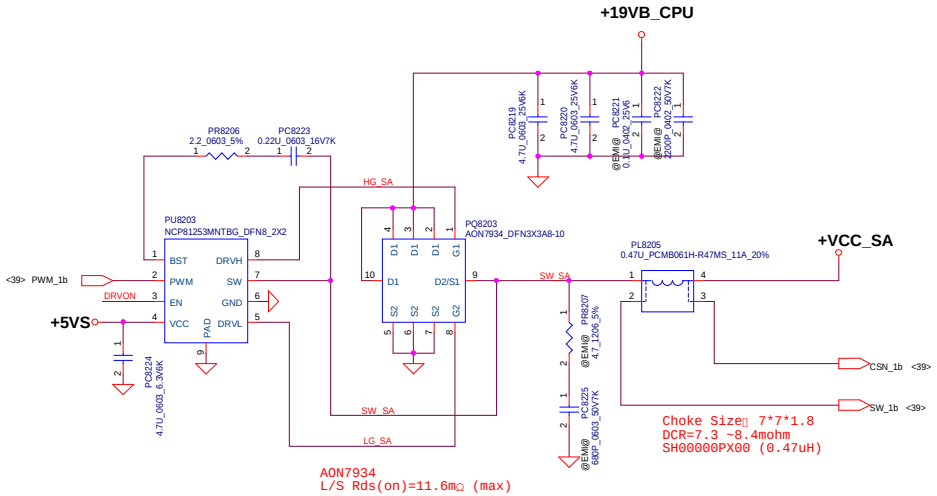


VCORE
Imax=21A Ipeak=29A Iocp=35A
LL=2.4mV/A

GT
Imax=18A Ipeak=31A Iocp=40A
LL=3.1mV/A

VCCSA
Imax=4A Ipeak=4.5A Iocp=9.5A
LL=10.3mV/A





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Issued Date	2015/1/15	Deciphered Date	2017/10/09

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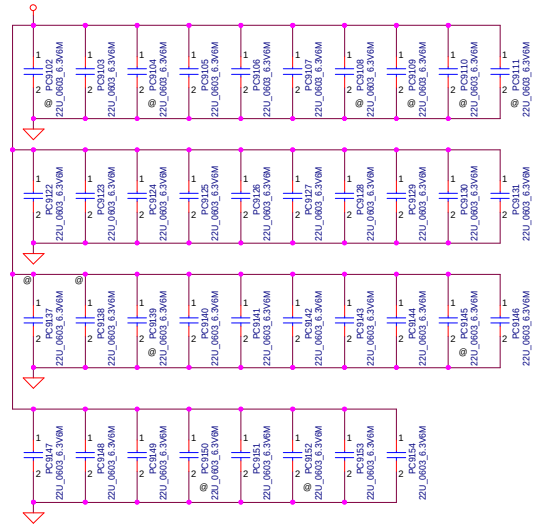
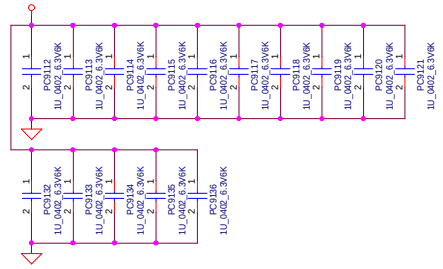
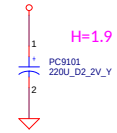
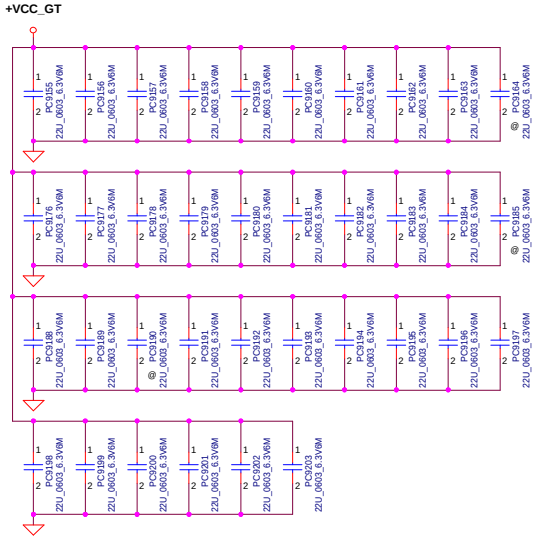
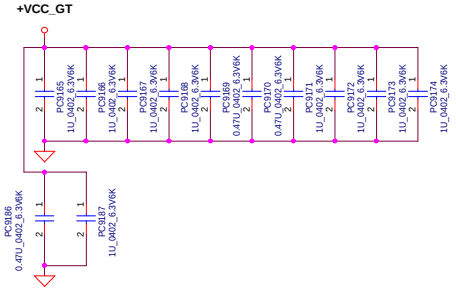
Compal Electronics, Inc.	
Title	CPU Poer Stages
Size	Document Number: LA-C482P
Rev	2.0
Date:	Wednesday, February 24, 2016
Sheet	40 of 43

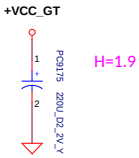


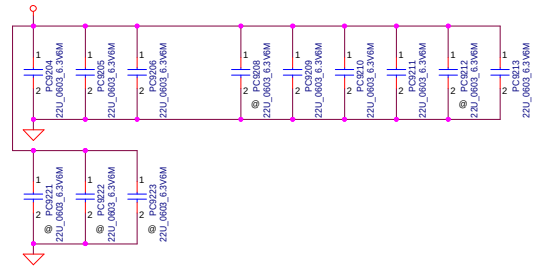


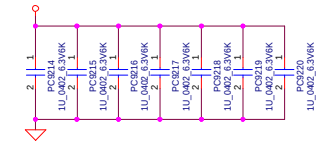












330U_D3_2.5VY_R6M-->H=1.4
SGA00006A00

330U_D2_2V_Y-->H=1.9
SGA00009S00

2015/09/15

VCORE Output Cap
22U 6.3V X5R 0603 * 38
1U 6.3V X5R 0402 * 15
330U 2.5V D2 ESR6M * 1

VCCGT Output Cap
22U 6.3V X5R 0603 * 36
1U 6.3V X5R 0402 * 12
330U 2.5V D2 ESR6M * 1

VCCSA Output Cap
22U 6.3V X5R 0603 * 13
1U 6.3V X5R 0402 * 7

2015/10/21

VCORE Output Cap
Backside
22U 6.3V X5R 0603 * 13
1U 6.3V X5R 0402 * 15

Primary
22U 6.3V X5R 0603 * 16

VCCGT Output Cap
Backside
22U 6.3V X5R 0603 * 13
1U 6.3V X5R 0402 * 9
0.47U 6.3V X5R 0402 * 3

Primary
22U 6.3V X5R 0603 * 20
220U 2V D2 * 1

VCCSA Output Cap
Backside
22U 6.3V X5R 0603 * 4
1U 6.3V X5R 0402 * 7

Primary
22U 6.3V X5R 0603 * 3

Security Classification	Compal Secret Data		
Issued Date	2015/1/15	Deciphered Date	2017/10/09

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Compal Electronics, Inc.

Title: **CPU DECOULPING**

Size	Document Number	Rev
	LA-C482P	2.0

Date: Wednesday, February 24, 2016 Sheet 41 of 43

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P36	change	11/19	Jims_Liu	avoid material shortage	PL502 change SH000015N00 to SH00000AA00	
2	P36	change	11/19	Jims_Liu	avoid material shortage	PU501 change SA000096O00 to SA00007IH00	
3	P37	change	11/19	Jims_Liu	for power efficient	PL602 change SH00000TV00 to SH000014Y00	
4	P41	POP	11/19	Jims_Liu	for CPU trancient	22uF (PC9107、PC9131、PC9140、PC9198、PC9199、PC9200) change unpop to SMT	
5	P41	non-POP	11/19	Jims_Liu	for CPU trancient	22uF (PC9190、PC9164、PC9185、PC9111,PC9145, PC9104,PC9108,PC9122,PC9123) change SMT to unpop	
6	P41	change	11/19	Jims_Liu	for CPU trancient	PC9101 change from SGA00009S00_330uF to SGA20221D40_220uF and SMT	
7	P39	non-POP	11/19	Jims_Liu	for CPU trancient	PR8130 change from SD014280380_280Kohm to SD014309380_309Kohm	
8	P39	change	11/19	Jims_Liu	for CPU trancient	PR8122 change form SD034261280_26.1Kohm to SD034240280_24Kohm	
9	P39	change	11/19	Jims_Liu	for CPU trancient	PR8123 change from SD034523180_5.23Kohm to SD034475180_4.75Kohm	
10	P39	change	11/19	Jims_Liu	for CPU trancient	PC8116 change from SE075472K80_4700pF to SE075222K80_2200pF	
11	P39	change	11/19	Jims_Liu	for CPU trancient	PR8114 change from SD034590280_59Kohm to SD00000H880_54.9Kohm	
12	P39	change	11/19	Jims_Liu	for CPU trancient	PC8106 change from SE000000680_8200pF to SE068103K80_0.01uF	
13	P39	change	11/19	Jims_Liu	for CPU trancient	PR8137 change from SD034178280_17.8Kohm to SD034158280_15.8Kohm	
14	P39	change	11/19	Jims_Liu	for CPU trancient	PR8152 change from SD00000CO80_590ohm to SD034576080_576ohm	
15	P39	change	11/19	Jims_Liu	for CPU trancient	PR8154 change from SD00000JJ00_665ohm to SD034576080_576ohm	
16	P38	change	11/19	Jims_Liu	change to common part	PL701 change from SH00000XB00 to SH000011S00	
17	P34	change	11/19	Jims_Liu	follow HW 2nd source	PQ301、PQ308 change from SB000009Q80 to SB00000ST00	
18	P39	change	11/24	Jims_Liu	Save production time	PR8139、PR8120 change from 0 ohm to R_short	
19	P37	change	11/24	Jims_Liu	for HW require	PR605 change from SD034137280_13.7K to SD00000QM80_14.3K	
20	P37	change	11/24	Jims_Liu	for audio noise	PC8219, PC8220 change from SE00000QK00_10uF to SE000013880_4.7uF	
21	P38	change	11/25	Jims_Liu	for PU701 pull high	PR701 change from SD028470280_47Kohm to SD028100480_1Mohm	
22	P39	change	11/27	Jims_Liu	co-lay	add PR8163_SD000005V00 co-lay 5Valw PR8194_SD000005V00 change to unpop	
23	P37	change	11/30	Jims_Liu	more place for CPU_GT	PJ601 change from JUMP_43X118 to JUMP_43X79	
24	P35	change	12/08	Jims_Liu	for efficiency	PL402 change from SH00000LT00_2.2uH_H1.5 to SH00000A900_2.2uH_H1.8	
25	P40	change	12/08	Jims_Liu	for efficiency	PL8205 change from SH000018B00_.47uH_H1.5 to SH00000PX00_.47uH_H1.8	
26	P34	change	01/11	Jims_Liu	for EMI request	remove unpop PL301(SH00000PB00) & PJ301	
27	P34	change	01/13	Jims_Liu	for power debug	add PJ301	

Security Classification: Compal Secret Data
Issued Date: 2015/1/15 Deciphered Date: 2017/10/09
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Compal Electronics, Inc.
Title: PWR-PIR
Size: D Document Number: LA-C482P Rev: 2.0
Date: Wednesday, February 24, 2016 Sheet 42 of 43

Version Change List (P. I. R. List)

Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	ALL	PWR	9/14		combine power schematic 0914	combine power schematic 0914	
2	P.20	HW	9/14		remove DDR cap	remove CD150,CD151	
3	ALL	HW	9/14		Compare connector list	Compare connector list	
4	P.24,25	HW	9/30		USB cap change to B2	CS12,CS25 chagne to SGA00009M00	
5	P.29	HW	9/30		remove for assembly change	Remove SW3,SW4	
6	P.23,26	HW	10/1		JUMP change to R-short for placemant	J1,J17 change to RM2,RA2	
7	P.23	HW	10/1		SATA cap chagne size for placement	CM7,CM8,CM9,CM10 change from 0402 to 0201	
8	ALL	HW	10/1		swap pin for layout routing	Swap LY1,LY2,LY3 LY4 ,LS5,LS4,LS12,RPC5	
9	P.26	HW	10/2		USB3 re-driver update P/N for new version	US5 change from SA00005OR00 to SA00005OR30	
10	P.28	HW	10/5		For KB/B debug	Add RK15,RK16	
11	P.26	HW	10/5		update FPC pin define	update JSB1 pin define	
12	P.9,11	HW	10/5		change Project_ID&RAM_ID pin	pin_U1-4 for RAM_ID , pin_P1-4 for Project_ID	
13	P.9,11	HW	10/5		Change USB30 ESD part for ESD request	Add DS5,DS6,DS8,DS10	
14	P.8	HW	10/7		EC schematic checklist	RPC1 chagne from 1k to 2.2k	
15	P.12	HW	10/7		for layout request	Swap RPC9,RPC10	
16	ALL	HW	10/7		For DFX/EMI request	Change LX2,LS4-LS12 from 0805 to 0504	
17	P.23	HW	10/7		For layout co-lay	Add RM16,RM17	
18	P.10	HW	10/7		Remove ME reset pad	Remove CC119,CLRP3	
19	P.10	HW	10/7		Add 60.4 PD for XTAL_BIASREF	Reserve RC158	
20	P.10	HW	10/7		update Crystal P/N	update YC1,YC2	
21	P.11	HW	10/7		Combine net to RPC8	Combine DGPU_PWR_EN to RPC8	
22	P.13	HW	10/7		Add Cap for load switch output	Add CC51	
23	P.14	HW	10/7		Non-DS3 sequence	Pop RC135 ; unpop RC137	
24	P.21	HW	10/7		Reduce 0ohm part count	Remove RX2,RX7	
25	P.23	HW	10/7		Change SSD power cap value	CM5 change from 4.7uF to 10uF	
26	P.8	HW	10/7		Combine parts	QC1 change to SB00000DH00	
27	P.25,28	HW	10/7		Combine parts	QG1,QS2 change to SB00000S700 (SOT323)	
28	P.28	HW	10/7		modify KB schematic	RK14 change to 1K , remove RK12,RK13	
29	P.29	HW	10/7		modify FAN schematic	Remove RF3	
30	P.30	HW	10/7		Add Cap for load switch output	Add CC53,CC55	
31	ALL	PWR	10/8		Combine power schematic 1008	Combine power schematic 1008	
32	P.25,28	HW	10/8		Combine parts	QG1,QS2 change to SB00000ST00	
33	P.29	HW	10/12		update screw hole	H24,H25,H26 change to PTH	
34	P.25	HW	10/13		combine USB into ESD diode	delete DS7,DS9 , USB into DS5,DS6,DS8,DS10	
35	P.25	HW	10/13		Change Type-C cap volt (6.3V&16V -> 25V)	Change CS26,CS29 to 25V	
36	P.27	HW	10/14		Add BT_ON on EC pin120	Add BT_ON on EC pin120	
37	ALL	HW	10/15		For EMI request	Remove CC10,CG2,CS8,LY1,LY2,LY3,LY4	
38	P.26	HW	10/15		update JSB1 pin define	USB_OC0# change to BT_ON	
39	ALL	PWR	10/15		Combine power schematic 1015	Combine power schematic 1015	
40	P.25	HW	10/15		update Type-C schematic	Remove CS26 , update JUSB2 pin define	
41	ALL	PWR	10/15		Combine power schematic 1015B	Combine power schematic 1015B	
42	P.27	HW	10/16		update EC pin define for KB backlight	pin27 <-> pin72	
43	P.26	HW	10/16		update JSB1 pin define	delete one GND pin , add +3VS_WLAN	
44	ALL	HW	10/19		remove test point	CFG10-15,T30,T6	
45	P.14	HW	10/19		add cap to +3VALW_DSW	Add CC86	
46	P.28	HW	10/19		remove 0ohm	remove RK10	
47	ALL	HW	10/19		Change 0-ohm to R-short for part count	RM11,RC122,RC124,RS12,RQ1,RQ2,RC49,RC81,RC83,RC111,RC115, RC113,RC114,RC125,RC127,RC128,RC131,RC132,RC134,RC136,RC144, RC145,RC118,RC119,RC123,RC126,RC133	
48	ALL	PWR	10/19		Combine power schematic 1019	Combine power schematic 1019	
49	ALL	PWR	10/20		Combine power schematic 1020	Combine power schematic 1020	
50	P.13	PWR	10/21		BOM update	pop RC112 , unpop UC8,CC49,CC43,CC45	
51	P.14	PWR	10/21		BOM update	pop RC129 , unpop RC130	

Security Classification	Compal Secret Data		
Issued Date	2015/10/21	Deciphered Date	2016/06/21

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Compal Electronics, Inc.

Title: HW P.I.R (1/3)

Size: Custom | Document Number: B3ZMS LA-D591P | Rev: 2.0

Date: Wednesday, February 24, 2016 | Sheet 43 of 45

Version Change List (P. I. R. List) Page 2/3 for HW

Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
52	ALL	PWR	10/22		combine power schematic 1021C	combine power schematic 1021C	
53	P.10	HW	10/22		part count	unpop RC85	
54	P.13	HW	10/22		power source cap added	pop CC45,CC49	
55	P.21	HW	10/22		use USB interface touchscreen	unpop RX10,RX11	
56	P.28	HW	10/22		LED interface update	pop RG5 ; unpop RG6,QG1	
57	P.8,9	HW	10/22		update BOM config	RC31 -> LPC@ , RC32 -> TPM@ , RC54 -> EMC@	
58	P.11,18,19	HW	10/22		update BOM config -> X76@	UV1-4,RC150-157	
59	P.3	HW	10/22		update BOM config -> CPU	QJ8Q@,SR2EU@,SR2EY@,QJKK@	
60	P.27	HW	10/22		update Board ID	RB6 change to 0ohm	
61	ALL	HW	10/23		2.2uF change Part Number to SD000008880	CC54,CC60,CD28,CD53,CD51,CD22,CD48,CD37,CD46,CD24,CD44,CD42	
62	P.11,12	HW	10/23		Part count reduce	unpop RC50,RC51,RC92,RC93,CC24,CC25,CC26,CC27,CC28,CC29,CC30,CC31	
63	P.25	HW	10/23		Part count reduce	unpop CS19,CW6,CC109,CC110	
10/21 A gerber		10/21 A gerber		10/21 A gerber	10/21 A gerber	10/21 A gerber	10/21 A gerber
64	P.7	HW	11/11		UC2 X1 code	UC2 change from SA00005U600 to SA00007UR00	
65	P.26	HW	11/11		US5 change symbol to TI (small thermal pad)	US5 change symbol to TI (small thermal pad)	
66	P.28	HW	11/11		LED pin error	swap LED1,LED2	
67	P.25	HW	11/11		Type-C schematic update for CC_UFP#	QS2 change from singal-N to dual-N	
68	P.25	HW	11/12		Type-C schematic update for VCC	CS29 change from 10uF to 0.1uF	
69	P.26	HW	11/16		move U3 redriver to S/B	remove US5 from M/B	
70	P.26	HW	11/16		Change BTB CONN. for cost	JSB1 vendor change to ENTERY	
71	P.26	HW	11/16		WLAN_PME# PU at M/B side	RM6 desgin in M/B side	
72	P.26	HW	11/17		update JSB1 pin define	reduce +5VALW*1 , add +VDDA*1	
73	P.25	HW	11/17		Combine BOM	DS12 change to SCA00002M00 (same as S/B)	
74	P.8,28	HW	11/17		Remove TPM schematic	Remove TPM schematic	
75	P.25	HW	11/17		update Type-C schematic	Replace RS36 by J17 ; unpop QS1,QS2,RS34,RS56	
76	P.11	HW	11/17		remove SCI Pull-up	Remove RPC8 pin1	
77	P.6	HW	11/17		SOC_OCC# connect to GND	SOC_OCC# connect to GND	
78	ALL	HW	11/18		part count reduce	RC129,RB17,RC112,RA11,RA12,RC35,RS30,RS31,RS32,RG3,RG11,RC84, RC104,RC106,RX4,RC140,RS22,RS23,RF1,RC110,RC135,RX12,RX13	
79	P.26	HW	11/18		part count reduce	RA13 remove	
80	P.28	HW	11/18		unpop test power button	unpop SW1	
81	P.27	HW	11/18		Board ID update	RB6 change from 0-ohm to 12KOhm	
82	P.27	HW	11/18		update EC GPIO table	KBL_EN change from pin27 to pin25	
83	P.27	HW	11/18		update EC GPIO table	remove EC_LID_OUT#	
84	P.7	HW	11/19		change net[SM_PG_CTRL] PU power	RC25 PU change from +3VALW to +3VS	
85	P.8	HW	11/19		part count reduce	unpop RC26,RC27,RC30	
86	P.9,26	HW	11/19		remove PCH DMIC signal	remove RA7,RA8,net[PCH_DMIC_CLK],net[PCH_DMIC_DATA]	
87	P.30	HW	11/19		change to correct location by naming rule	CC53,CC55 change to CQ5,CQ6	
88	P.13	HW	11/19		combine parts -> 0.1uF 0201	CC46 change from 0402 to 0201	
89	ALL	HW	11/19		combine parts -> 10uF 0603	CC106,CS19,CS20,CS37	
90	P.26	HW	11/25		Use dual U3 re-driver for U3 issue	US5 group on M/B	
91	P.26	HW	11/26		Add AC cap between 1st 8713 & 2nd 8713	Add CS33,CS34	
92	ALL	PWR	11/26		Combine power schematic	Combine power schematic	
93	P.6	HW	11/26		Intel Debug	RC6,RC7,RC8,RC19 change t DCI@ (unpop)	
94	P.26	HW	11/26		update JSB1 pin define for EMI request	pin8 <-> pin60	
95	P.6	HW	11/26		reserve PU +3VS for EC_SCI# (for kabylake?)	Reserve RC159	
96	P.26	HW	11/27		Vendor recomment : update REXT PD value	RS53 change from 3.83k-ohm to 4.99k-ohm	
97	ALL	PWR	11/30		Combine power schematic	Combine power schematic 1130	
98	P.10	HW	12/1		Add PD for PLT_RST_BUF#	Add RC53	
99	P.26	HW	12/2		Remove U3 re-driver	Remove US5 group	
100	P.29	HW	12/2		Add PU for Thermal sensor SMBus	Add RPF1 , remove RF5	
101	P.27	HW	12/2		Add BOM config for ENE request (PLT_RST# PD)	RB5 100K for LPC@ , 47K for ESPI@	
102	P.28	HW	12/2		remove debug KB pin	remove RK15,RK16	

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Version Change List (P. I. R. List) Page 2/3 for HW

Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
103	P.13	HW	12/3		change load switch CT value	CC39 change from 10pF to 470pF	
104	ALL	PWR	12/8		Combine power schematic 1208	Combine power schematic 1208	
105	P.26	HW	12/31		Add PME PU on M/B	Add RM6	
106	P.14	HW	12/31		Cost reduce	unpop UC10,CC112	
107	P.29	HW	1/5		Add POA schematic	Add POA schematic	
108	P.28	HW	1/11		Change Battery LED power source to +5VALW	unpop RG3 ; pop RG2	
109	ALL	PWR	1/13		Combine power schematic 0111	Combine power schematic 0111	
110	P.13	HW	1/13		Factory issue	unpop CC52	
111	P.28	HW	1/18		LED R-value change	RG7->680ohm ; RG8->220ohm	
112	P.3	HW	1/19		Add Kabylake CPU P/N	Add SA00009QM10,SA00009PJ30	
113	P.27	HW	1/19		update project ID	RB6 change from 12K-ohm to 15K-ohm	
114	P.29	HW	2/15		update screw hole	H4 change from 2P8 to 3P2	
115	P.27	HW	2/15		update project ID	RB6 change from 15K-ohm to 20K-ohm	
116	P.29	HW	2/17		reserve 0-ohm for FP USB signal	reserve RK13,RK15	
117	P.28	HW	2/18		Combine Part Number	RG8 change from SD034220080 to SD028220080	
118	P.28	HW	2/19		LED value change	RG1 1.1k -> 1.6k ; RG4 1.6k -> 1k	
119	P.28	HW	2/19		HDMI/HDCP test result	RY11 change from 4.99k-ohm to 4.75k-ohm	
120	P.29	HW	2/19		update BOM config	RK10 change to FP@	
121	P.27	HW	2/19		update BOM config	Add RB6=56K for Kabylake	

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